AL250/251 Application Notes

Application Notes

Using the AL250EVB Evaluation Board

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1.0 Introduction

The AL250 Video Scan Doubler (De-Interlacer) is a video conversion chip for consumer video and multimedia applications. It converts interlaced NTSC and PAL digital signals into non-interlaced VGA signal for direct connection to a computer monitor or a progressive scan TV. The AL251 has all the functionality of the AL250 and additional digital YUV/RGB output for digital video processing and LCD panel applications.

Depending on the input format, the external circuits needed to cope with the AL250/251 vary. If the input is digital interlaced RGB or YUV, the AL250/251 alone with simple reference voltage circuits will suffice. If the input is analog interlaced composite or component video signal, a digital video decoder (which may require a micro controller) is needed for the decoding. If the input signal is in CATV or other similar formats, a TV tuner module is needed additionally. If closed caption or teletext is to be provided, then a caption decoder and certain OSD controller circuits may be required.

The AL250EVB converts analog interlaced composite/component NTSC/PAL signals to non-interlaced RGB outputs for VGA monitors. The decoder used is either SAA7110awp or SAA7111wp. The micro controller chosen is an 8051 with 4k bytes internal memory.

The AL250EVB provides the following:

- Demonstration of high-quality TV-to-VGA scan-conversion. (See the AL250/251 Data Sheets for full details).
- Toggle between component (S-video) and composite video.
- Auto detection (with SAA7111) or toggle between NTSC and PAL (with SAA7110).
- Internal OSD (on-screen display) bitmap demonstration.
- LUT (look up table) for color enhancement (gamma correction, etc.).
- Special effects (negative film, color filter, digitized effects, etc.).
- Stand-alone board application.
- Single +5V operation.

2.0 Using the AL250/251

The AverLogic AL250/251 is a highly integrated IC consisting of scan doubler circuits, memory, look up table, proprietary digital signal processing, overlay control circuits and three high speed D/A converters all within a 64-pin (AL250) or 80-pin (AL251) QFP package.

Although the AL250/251 is designed to be plug & play (note: the decoder IC may not be), the 48 internal registers and 1k byte internal RAM provide the AL250/251 with many programmable features. Details can be found in the Register Definition section of the AL250/251 Data Sheets. The functions can be controlled by dedicated hardware pins as well as by software. The I^2C interface provides full software programmability. Some of the features can easily be demonstrated by using the push buttons on the EVB, although they are optional and customers may choose not to use them in product designs because of cost considerations. Details of the push buttons functionality can be found in the Switch Settings section.

2.1 Additional Circuits for the DAC

The compensation pin (COMP) is pulled up with a 0.1µF capacitor. The voltage reference input (VREF) is set at 1.23V exactly by a voltage reference chip such as a LM385 so that the power plane or fluctuation does not affect the video output. A 0.1uF capacitor is applied in parallel to further ensure the stability of the reference voltage. The RSET pin is pulled down to ground with a resistor of 150ohm for appropriate VGA output voltage level. The resistance values may need to be adjusted to compensate for the impedance mismatch and signal attenuation for circumstances such as long cables.

2.2 I^2C Programming

The AL250/251 I^2C programming interface follows the Philips standard. The I^2C interface consists of the SCL (clock) and SDA (data) signals. Data can be written to or read from the AL250/251. For both read and write, each byte is transferred MSB first, and the SDA data bit is valid when the SCL is pulled high.

The read/write command format is as follows:

Write: <S> <Write SA> <A> <Register Index> <A> <Data> <A> <P>

Read: <S> <Write SA> <A> <Register Index> <A> <S> <Read SA> <A> <Data> <NA> <P>

Following are the details:

<**S**>:
Start signal

SCL	SDA
High	High
High	Low

The Start signal is HIGH to LOW transition on the SDA line when SCL is HIGH.

<**WRITE SA**>:
Write Slave Address: 58h or 5Ch

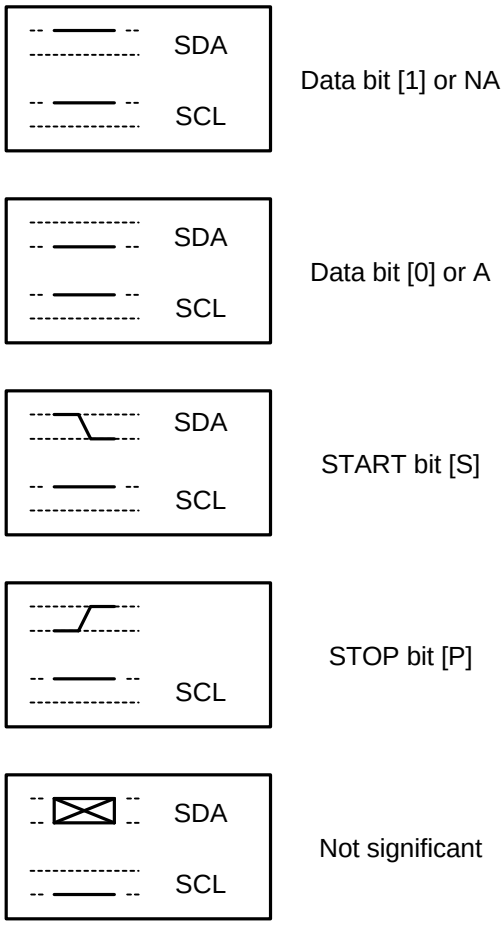
<**READ SA**>:
Read Slave Address: 59h or 5Dh

<**REGISTER INDEX**>:
Value of the AL250/251 register index.

<**A**>:
Acknowledge stage
The acknowledge-related clock pulse is generated by the host (master). The host releases the SDA line (HIGH) for the AL250/251 (slave) to pull down the SDA line during the acknowledge clock pulse.

<**NA**>:
Not Acknowledge stage
The acknowledge-related clock pulse is generated by the host (master). The host releases the SDA line (HIGH) during the acknowledge clock pulse, but the AL250/251 does not pull it down during this stage.

<**DATA**>:
Data byte write to or read from the register index.
In read operation, the host must release the SDA line (high) before the first clock pulse is transmitted to the AL250.



AL250-15 I2C drawing

<**P**>:
Stop signal

SCL	SDA
High	Low
High	High

The Stop signal is LOW to HIGH transition on the SDA line when SCL is HIGH.

2.3 Video Decoding

A video decoder (video input processor) is needed with the AL250/251 for S-video or composite video processing. Please note that the AL250/251 works only with line-locked video decoders.

There are a number of video decoders available in the market; following is a selection chart. For detailed information, please consult with the decoder vendors or their distributors directly. The attached information is believed to be accurate but not guaranteed.

Decoder	Vendor	Line locked	NTSC/ PAL	RGB565	CCIR 601	Square Pixel	Closed Caption	Tele text
SAA 7110	Philips	V	V			V		
SAA 7111	Philips	V	V	V	V			
SAA 7112	Philips	V	V	V	V			
KS0127	Samsung	V	V	V	V		V	
VPC3211B	ITT	V	V		V			V

2.4 Resolution

The resolution of the AL250/251 applications depends on the input video source, e.g., the digital video decoder. The typical resolution of the video decoders is as follows:

	Square pixel		CCIR 601	
	NTSC	PAL	NTSC	PAL
Pixel Total	780 x 525	944 x 625	858 x 525	864 x 625
Pixel Active	640 x 480	768 x 576	720 x 480	720 x 576

The AL250/251 can process up to 768 active pixels per line and 1024 lines per frame.

2.5 Border/Border Color

The AL250/251 displays all of the active pixels from the video source resulting in a larger viewable area on a monitor than on a regular TV. This is especially advantageous for digital video sources such as DVD. However, for some other video sources such as VCR, the unwanted and untrimmed border may appear. To solve this, the AL250/251 provides border control by cropping the video source. In addition, the cropped border can be filled with one color (24-bit), which is defined by registers 0Ch~0Eh.

Border/border color control applies to the AL250/251 analog output but not to the AL251 digital YUV/RGB output.

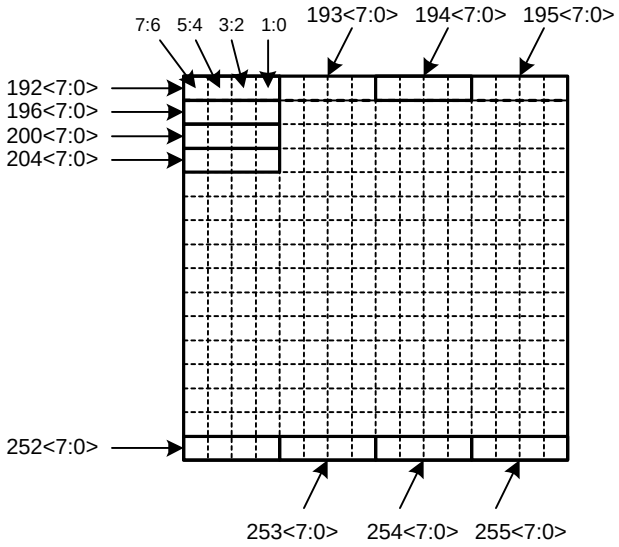
2.6 OSD Interface

The AL250/251 provides two ways to implement the on screen display. The internal way is to program the built-in on-screen display (OSD) bitmap, and the external way is to control the two overlay pins for showing on screen display or creating special effects onto each single pixel on screen. The AL250/251 provides 256 registers to implement the two internal bitmaps, which are programmable as 16x16 blocks (4x4 pixels each) and 48x16 blocks (8x8 pixels each) respectively.

To program the OSD, first use LUT/OSD Control register 10h to turn on bitmap 1 or bitmap 2. Then program the overlay colors 1, 2 and 3 through registers 15h~1Dh. Select the OSD index (0~255) through register 11h, then fill the data through register 13h. The two bits of each OSD

block can be used to define no overlay color (transparent) or color 1, 2 or 3. Mesh color and mesh background can be enabled by programming register 2Fh. The position of the bitmaps can be defined by registers 1Eh, 1Fh, and 2Fh.

The data index of the bitmap 1 starts at bitmap address 192, and the lay-out is defined as follows:



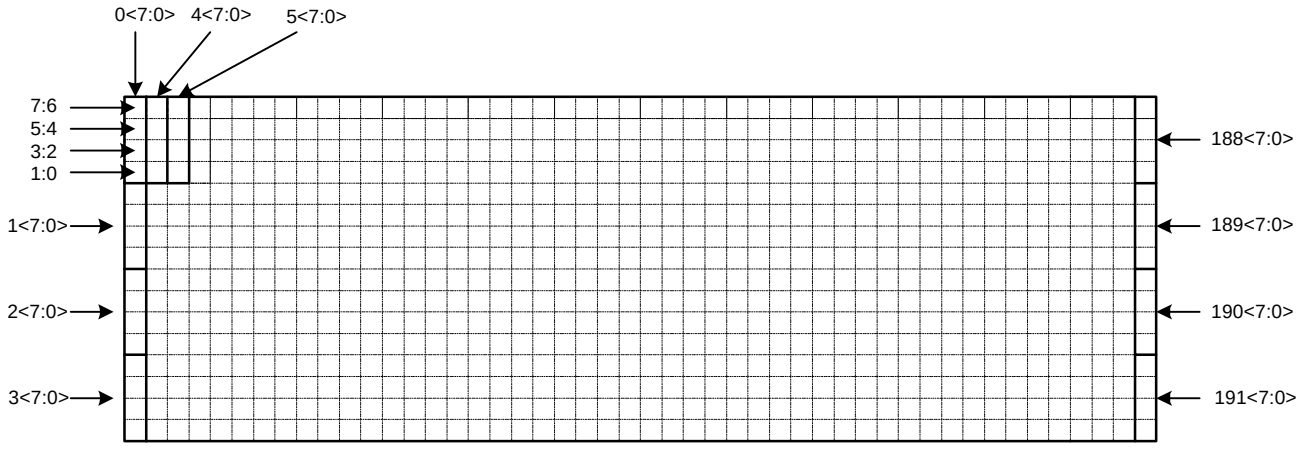
AL250-16
16x16 OSD drawing

Each pixel is defined by 2 bits value (“00”, “01”, “10” and “11”).

Value “00” shows the current input video data.

Value “01”, “10” and “11” are index to overlay color 1~3 (defined in registers 15h ~ 1Dh).

The data index of bitmap 2 starts at bitmap address 0, and the lay-out is defined as follows:



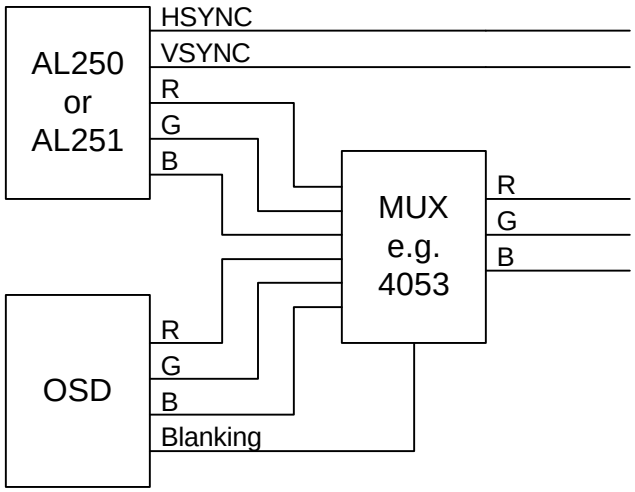
AL250-17 16x48 OSD drawing

Similar to bitmap 1, each pixel is defined by 2 bits value (“00”, “01”, “10” and “11”) with the same definition.

The horizontal positions of the bitmaps 1 & 2 are defined by registers 1Eh and 1Fh respectively. The vertical position of both is defined by register 2Fh.

The internal OSD control applies to the AL250/251 analog output and the AL251 digital RGB output, but not to the AL251 digital YUV output.

For the external OSD, the overlay feature can be used, which will be explained in detail in the External Overlay section. For applications such as closed caption or Teletext display, the OSD or Overlay function of the AL250/251 may not be ideal. A dedicated OSD chip or a caption decoder with OSD functionality may be more cost effective. If the selected external OSD chip does not support an input port for multiplexing the OSD output with the AL250/251analog output, adding a simple MUX chip would suffice. The multiplexing circuitry can be used as follows:



AL250-18 External OSD

2.7 External Overlay

The AL250/251 provides two overlay pins (OVLCTRL1 and OVLCTRL0) for overlay control as well as some special effects. They can be pulled as 00 for no overlay, and 01, 10, 11 for different overlay colors or effects. The colors can be chosen from any one of 16M colors (defined by 24 bits RGB) by programming registers 15h~1Dh. The effects can be logic AND, OR, or XOR of the video source with any of the three overlay colors by programming register 14h. For instance, a negative film effect can be produced by the XOR as a result of the original video source and white color. More details can be found in the Register Definition section of the AL250/251 Data Sheets.

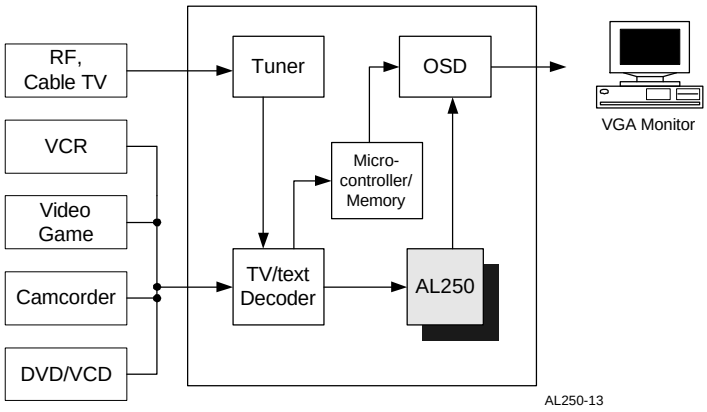
Using the external overlay of the AL250/251 for caption display is possible if the OSD or FPGA chip chosen for displaying fonts of the decoded caption has the two overlay pins compatible with the AL250. If not, then the digital or analog output of the OSD can still be multiplexed with the output of the AL250/251 to show captions on the video display as described in the OSD Interface section.

External overlay applies to the AL250/251 analog output and the AL251 digital RGB output, but not to the AL251 digital YUV output.

2.8 Caption Display

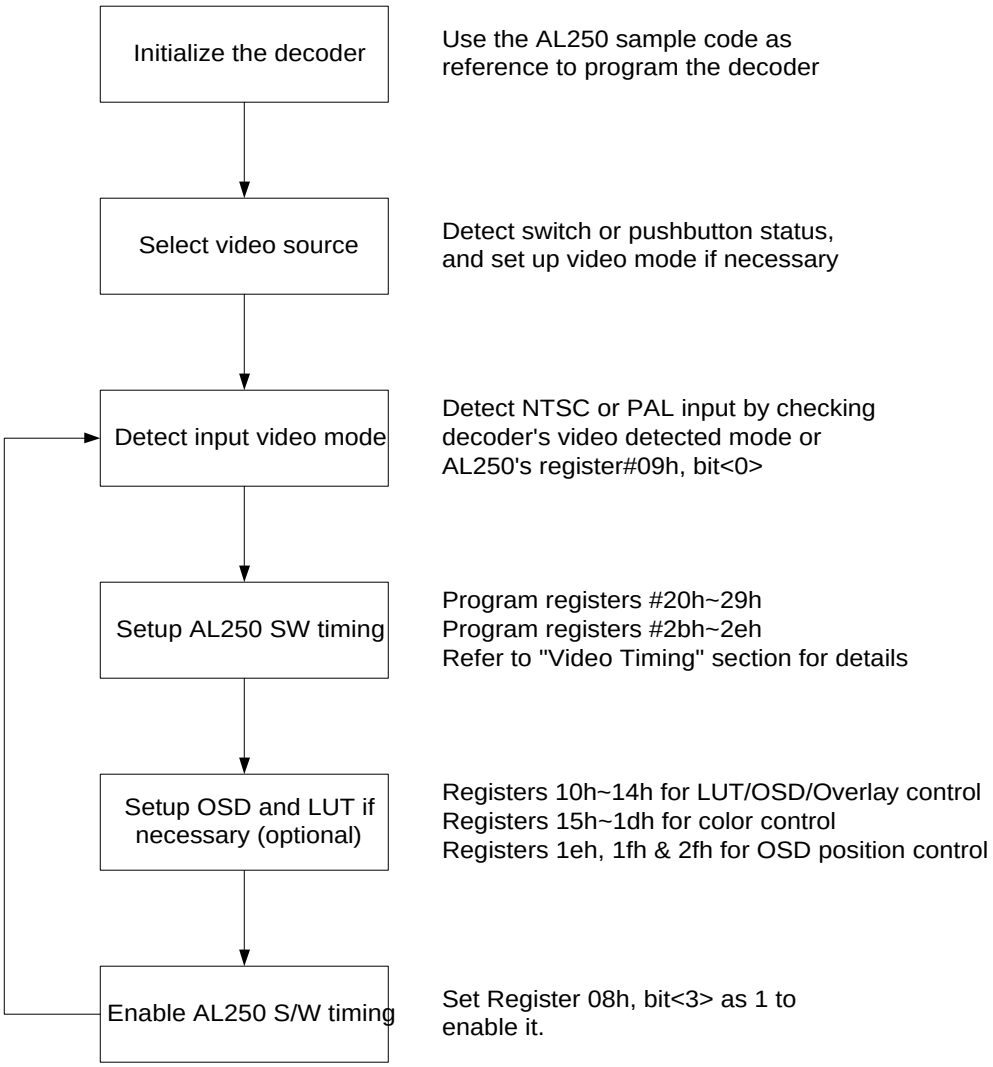
There are two ways to implement a caption display. One is to use a video decoder that is capable of caption decoding and the decoded caption is overwritten in the video data before being sent to the AL250/251. This is the most economic way of implementing caption display and is highly recommended.

If the video decoder does not provide caption decoding, or decoded caption signal is not in the two-pin overlay control format that the AL250/251accepts, then certain interface is needed. An economic way is to use a micro controller to read the decoded caption data from a caption decoder, arrange it, and write it to an OSD chip. The block diagram is as follows:



2.9 Programming Flow Chart

The following programming flowchart is for your reference. Details about the AL250 S/W timing can be found in the “Video Timing” section of the AL250 Data Sheets.



AL250-21 Programming Flow Chart

2.10 Using the Digital RGB/YUV output (AL251 only)

In addition to analog RGB output, the AL251 also provides digital output in RGB565 or YUV422 format. The pin definition and the RGB565-888 mapping is as follows:

Video Data Signal	Pin #	YUV 422	RGB 565→888
DO7	56	Y7	R7
DO6	55	Y6	R6
DO5	52	Y5	R5
DO4	51	Y4	R4
DO3	50	Y3	R3

DO2	49	Y2	G7
DO1	48	Y1	G6
DO0	47	Y0	G5
DO15	66	U7, V7	G4
DO14	65	U6, V6	G3
DO13	64	U5, V5	G2
DO12	63	U4, V4	B7
DO11	26	U3, V3	B6
DO10	25	U2, V2	B5
DO9	24	U1, V1	B4
DO8	23	U0, V0	B3
OutFormat select	-	1	0

To select YUV422 or RGB565 as output format, program the Control Register #08h<7>, i.e., OutFormat. The Overlay, OSD, LUT and border control do not apply to the digital YUV output. The LUT and border control do not apply to the digital RGB output.

2.11 "No-video" Detection

Some decoders do not send HSYNC signal when there is no input so the AL250 may not send output HSYNC properly (such as KS0127). Some decoders may generate background noise when there is no input and such noise may be undesirable. In either case, no-video detection may be necessary and following is the suggestion:

For the first case, H-lock or NOVIDEO status needs to be detected (usually available in the "status" register). When there is such "no input video" status detected, set the decoder to perform free running to generate HSYNC automatically. Note that after setting the decoder in free running mode, the decoder may automatically write H-lock status as 1 again, thus forbidding actual input video from being detected again. For details, please consult with your decoder vendor.

For the second case, also detect the H-lock status. When there is no H-lock, turn on the overlay control of the AL250, and AND the background with a color black, or OR the background with a color blue to eliminate the output noise. Refer to "Overlay Control" section for more details.

For your reference, the H-lock information can be read from register 1Fh, bit 6 of SAA7111, or register 00h, bit 1 of KS0127. Free running mode can be set at register 03h, bit 7 of KS0127. The SAA7111 provides automatic free-running output.

2.12 Power Consumption

The AL250/251 works at both 5V and 3.3V. The following table shows the current consumption of the AL250/251 itself and that of the whole EVB with power supply at single 5V, or 5V and 3.3V mixed (3.3V for the AL250 only).

	+5V	+3.3V for AL250 +5V for the rest
AL250/251chip	92 mA (typ.)	55 mA (typ.)
AL250 EVB	280 mA (typ.)	140 mA (typ.)

Please be reminded that when lower power supply is used, the pull-down resistance to the RSET pin has to be adjusted to compensate accordingly. The lower the supply voltage is, the lower the pull-down resistance has to be. The ideal resistance values can be achieved by adjusting the RGB output to be 0.7V peak-to-peak.

3.0 Board Design and Layout Considerations

The AL250/251 contains both precision analog and high-speed digital circuitry. Noise coupling from digital circuits to analog circuits may result in poor video quality. The layout should be optimized for lowest noise on the power and ground planes by shielding the digital circuitry and providing good decoupling.

It is recommended to place the AL250/251 chip close to the VGA output connector, and the video decoder close to the analog video input connectors if applicable.

3.1 Grounding

Analog and digital circuits are separated within the AL250/251 chip. To minimize system noise and prevent digital system noise from entering the analog portion, a common ground plane for all devices, including the AL250/251 is recommended. All of the connections to the ground plane should have very short leads. The ground plane should be solid, not cross-hatched.

3.2 Power Planes and Power Supply Decoupling

The analog portion of the AL250/251 and any associated analog circuitry should have their own power plane, referred to as the analog power plane (AVDD). The analog power plane should be connected to the digital power plane (DVDD) at a single point through a low resistance ferrite bead.

The digital power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all of the AL250/251 analog power pins and relevant analog circuitry.

Power supply connection pins should be individually decoupled. For best results, use 0.1µF ceramic chip capacitors. Lead lengths should be minimized. The power pins should be connected to the bypass capacitors before being connected to the power planes. To control low-frequency power ripple, 22µF capacitors should also be used between the AL250/251 power planes and the ground planes.

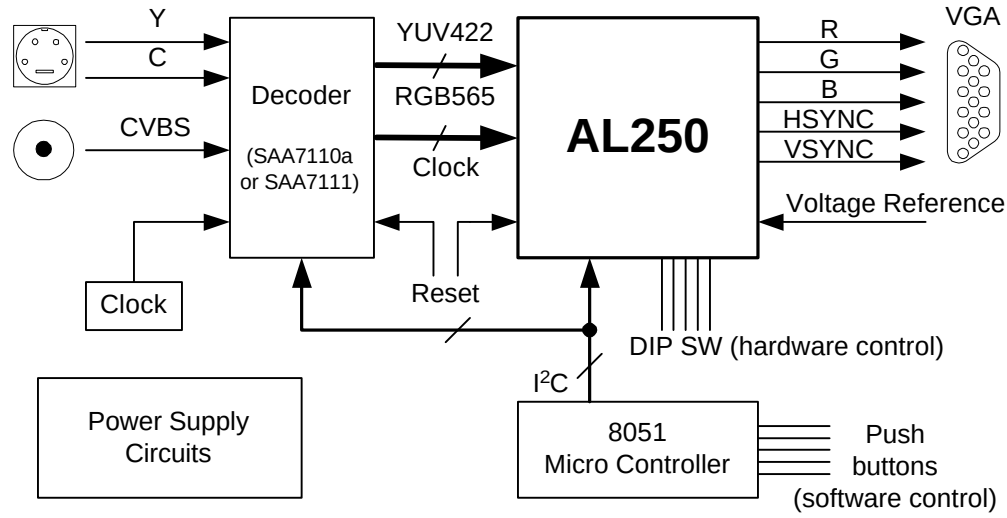
3.3 Digital Signal and Clock Interconnect

Digital signals to the AL250/251 should be isolated as much as possible from the analog outputs and other analog circuitry. The high frequency clock reference or crystal should be handled carefully. Jitter and noise on the clock will degrade the video performance. Keep the clock paths to the decoder as short as possible to reduce noise pickup.

3.4 Analog Signal Interconnect

The AL250/251 should be located closely to the output connectors to minimize noise and reflections. Keep the critical analog traces as short and wide (20~30 mil) as possible. Digital signals, especially pixel clocks and data signals should not overlap any of the analog signal circuitry and should be kept as far apart as possible. The AL250/251 and the decoder IC should have no inputs left floating.

4.0 Block Diagram and Settings



AL250-05 AL250EVB Block Diagram

4.1 Connector Description

Reference	Description
CON 1	S-Video connector (input)
CON 2	RCA-Jack Composite Video connector (input)
CON 3	DC 9V Power Jack
J1 (Optional)	Digital power connection (always shorted)
J2	VGA connector (output)
JP1 (Optional)	Clock test pins (VCLK, VCLKX2, VIDHS, VIDVS, and HREF)
JP2	SAA7110/7111 select
JP3 (Optional)	Test pins (for factory test only)

4.2 LED Definition

Reference	Description
D3 (Green LED)	Power-on indicator

4.3 Switch Settings

Reference	Name	Description
S1-1	U/V Flip	To keep U/V correct, keep this switch always ON. (Note: the silk screen on the EVB is incorrect)

S1-2	CCIR Select	CCIR601/Square Pixel select On: Square pixel Off: CCIR601
S1-3	422/565 Select	YUV422/RGB565 select On: RGB565 Off: YUV422
S1-4, 1-5	NTSC/PAL Select	NTSC/PAL input select (hardware control) 00: NTSC 01: PAL 10: Auto detection 11: Reserved
S2	Micro Reset	Reset push button for the micro controller. After reset, it takes 5 seconds to be ready for any instructions from the push buttons.
S3	Video Source	Toggle between S-video and composite video
S4	NTSC/PAL	Toggle between NTSC and PAL (software control)
S5	OSD	On screen display for the two internal bitmaps. Toggle to show bitmaps, bitmaps with mesh effect, and no bitmaps.
S6	LUT	Toggle to turn on and off the internal look up table for gamma correction.
S7	Effects	Special effects. Toggle among negative effect, red, green, blue filter effects, and digitized effect.
S8	Border	Toggle among black border (default), red, green, blue yellow borders, and no border.
S9	AL250 Reset	Reset pushbutton for the AL250 and the decoder
S10	Enhancement	Toggle between further enhancement of LUT (higher contrast) and default value of LUT. S6 needs to be ON to show the difference.
S11	Home	Resume default settings of the software control.

Remarks:

- The AL250EVB Ver. B does not demonstrate the external overlay control. To see the whole functionality of the AL250, please review the AL250EVB Ver. A.
- When TESTIN pin (controlled by S1-1) is not pulled high, U/V may flip and the output color may be incorrect.

5.0 Schematics

Two pages of schematics are available upon request.

5.1 Bill of Materials

Item	Q'ty	Reference	Part
1	1	CON1	S Video Connector
2	1	CON2	RCA Jack
3	1	CON3	Power Jack
4	4	C1,C6,C25,C30	22uF
5	3	C2,C5,C14	0.01uF
6	20	C3,C4,C7,C8,C9,C10,C11,C12,C13,C19,C26, C27,C28,C29,C31,C32,C33,C34,C35,C39	0.1uF
7	8	C15,C16,C17,C18,C21,C22,C23,C24	10pF
8	1	C20	1000pF
9	5	C36,C38,C40,C41,C42	1uf (opt)
10	2	C51,C37	10uF
11	2	C52,C44	1uF
12	2	C47,C46	20pF
13	1	D1	1N4148
14	1	D2	1N5822
15	1	D3	Green LED
16	1	F1	1A Fuse
17	1	JP2	Short 2 of the 3 pads
18	1	J1	Shorted
19	1	J2	VGA Connector
20	4	L1,L2,L3,L4	FB
21	1	L5	10uH
22	1	L6	Ferrite Bead
23	1	RN1	10K Net 8
24	1	RN2	470 Net 9
25	6	R1,R2,R3,R4,R5,R8	75
26	1	R6	27K
27	1	R7	150
28	3	R9,R13,R14	4.7k
29	1	R10	1K
30	1	R11	470
31	2	R15,R12	10K
32	1	R16	300
33	1	R17	1M

34	1	R18	750
35	1	S1	SW DIP-5
36	2	S2,S9	Push buttons
37	5	S3,S4,S5,S6,S7	Push buttons (Opt)
38	8	TP1,TP2,TP3,TP4,TP5,TP6,TP7,TP8	Shorted in pairs
39	1	U1	SAA7111
40	1	U2	AL250
41	1	U3	LM385-1.2
42	1	U4	80C51 PLCC
43	1	U5	LM7805
44	1	Y1	24.576 MHz
45	1	Y2	12 MHz

For more information about AverLogic products, please contact Averlogic Technologies, Inc. as provided in the Contact Information page.

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