AN-AL251A-EVB-A0-01

Hardware Application Notes for
AL251A-EVB-A0

Preliminary 0.1

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AN-AL251A-EVB-A0-01 Hardware Application Notes

Contents:

1 Introduction

The AL251A-EVB-A0 is an engineering evaluation board that is used to evaluate and demonstrate the performance of the AL128 VGA to TV scan converter chip and AL251 TV to VGA scan converter chip. The board contains two 3M bits of field memory (AL422B) for AL128, and one video decoder (AL242) for AL251. An attached 80C51 microcontroller is used to control AL242 and AL251 via 2-wire Serial Bus.

The evaluation board accepts VGA analog signals or analog video signals. AL128 converts the analog VGA signal into NTSC/PAL S-video and composite video (CVBS), or analog RGB for SCART application. Additional bypass VGA output could be added via the video buffer. This implementation can display at both the monitor and TV simultaneously. Through AL251 and AL242, it accepts NTSC/PAL S-video or composite video (CVBS) and converts into VGA analog signal output or 16-bits digital RGB/YUV output.

Various switches and buttons are designed in the evaluation board for ease of demonstrating and testing the functions. For detailed descriptions of each connector, button and LED, please refer to “Block diagram and settings” section.

The board uses an external DC power adaptor (+12V/1A).

2 Block Diagram

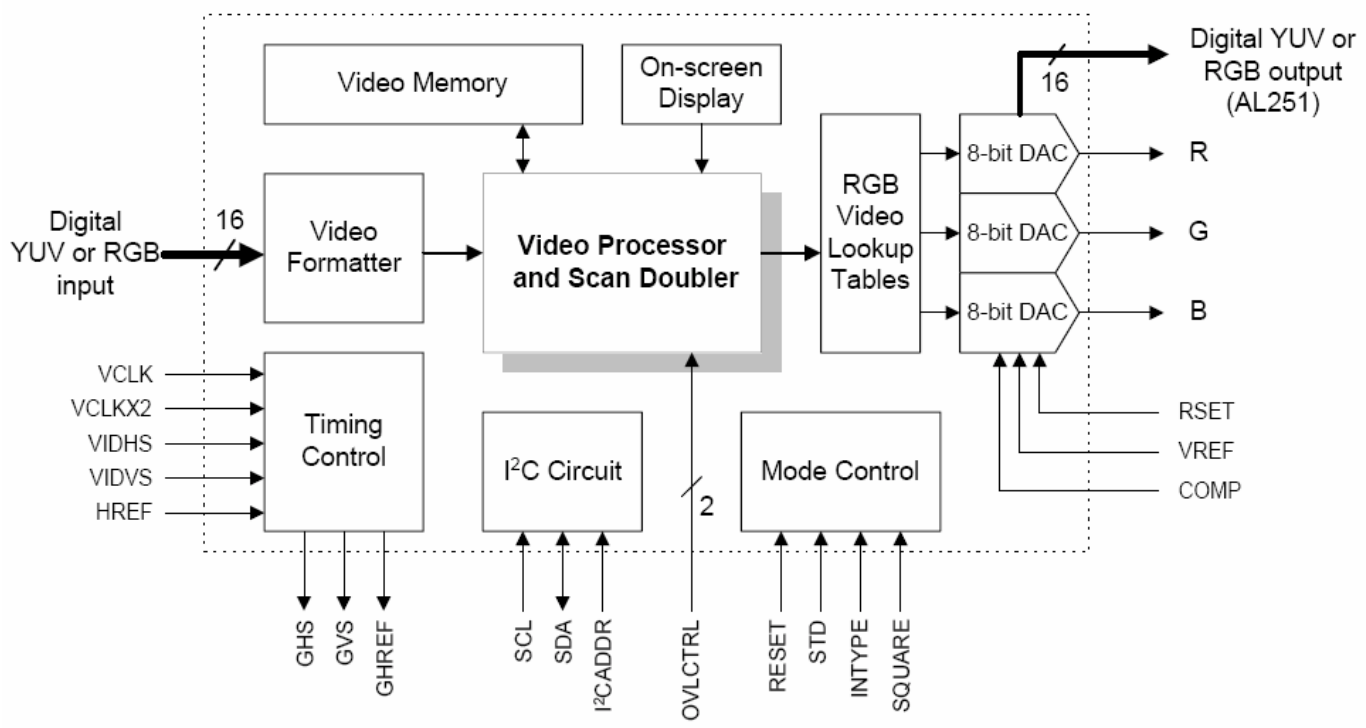


Figure 1: AL251 Functional Block Diagram

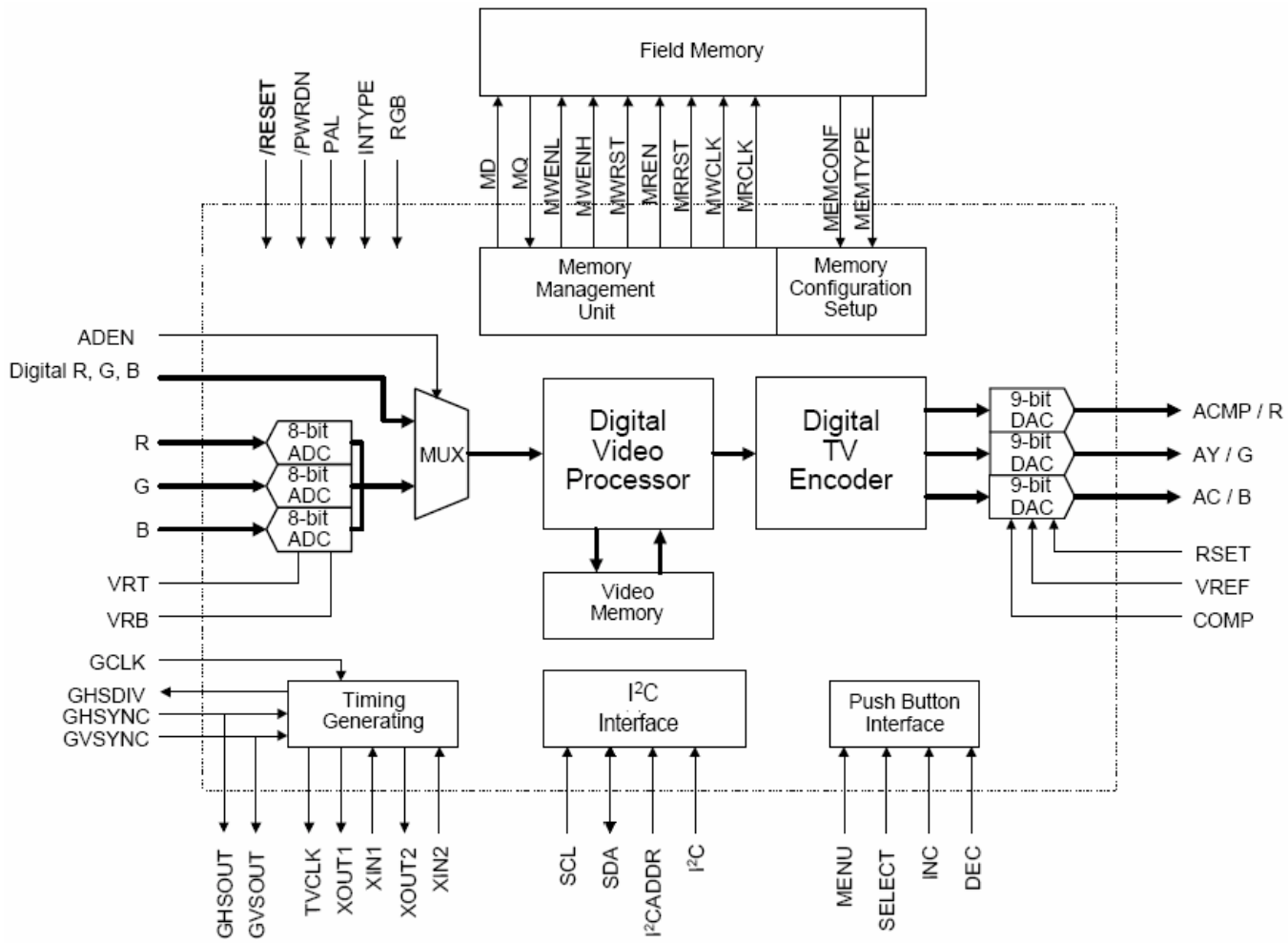


Figure 2: AL128 Functional Block Diagram

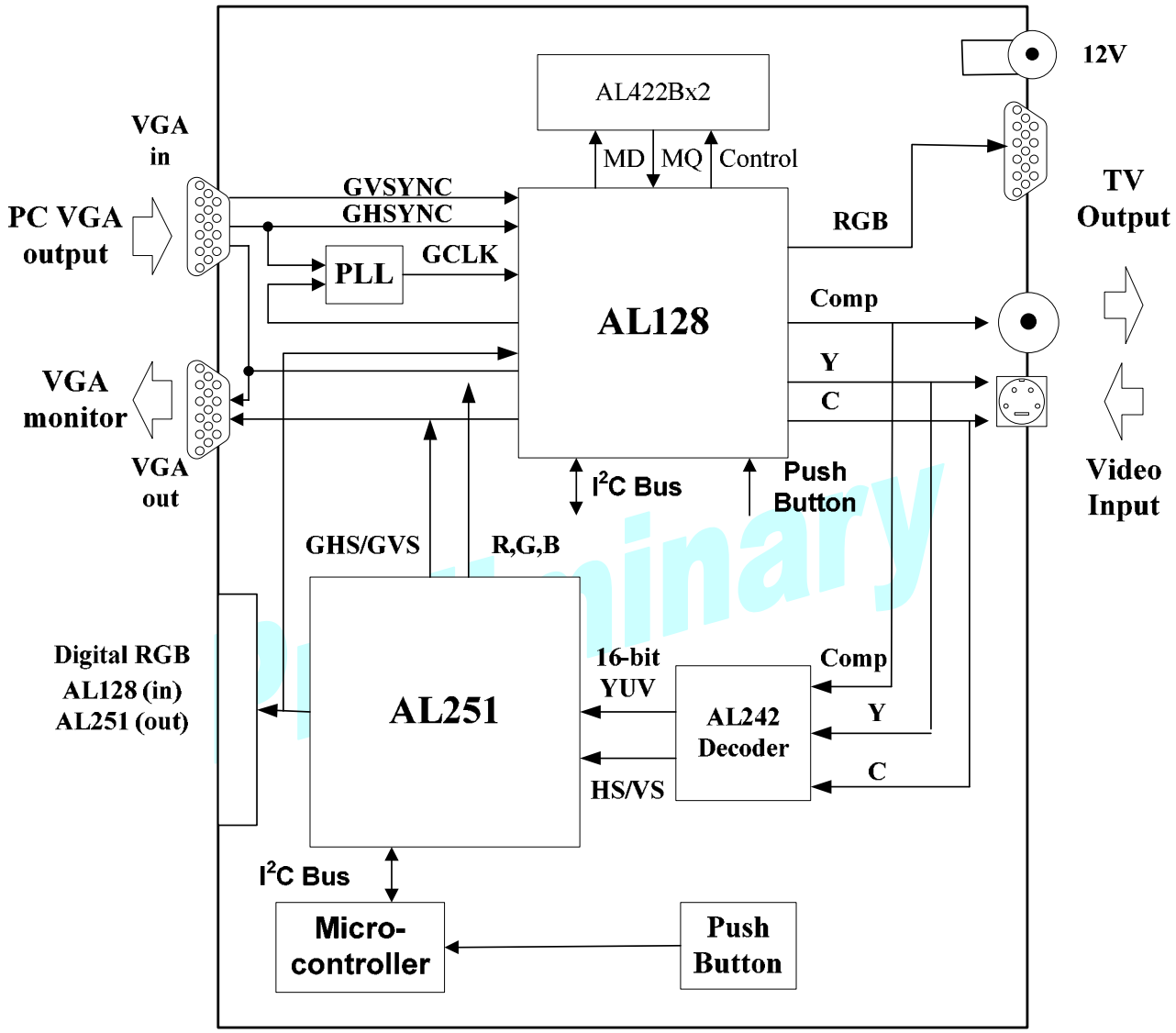


Figure 3: AL251A-EVB-A0 Functional Block Diagram

3 Video Input Formats

3.1 AL251 Video Input Formats

The digital video data formats that the AL251 accepts are YUV422 and RGB565. The pin definition and the RGB 888 to 565 mapping are as follows:

Video Data Signal	Pin Number	YUV 422	RGB 565
VDIN15	79	Y7	R7
VDIN14	78	Y6	R6
VDIN13	77	Y5	R5
VDIN12	76	Y4	R4
VDIN11	74	Y3	R3
VDIN10	73	Y2	G7
VDIN9	72	Y1	G6
VDIN8	70	Y0	G5
VDIN7	69	U7, V7	G4
VDIN6	68	U6, V6	G3
VDIN5	67	U5, V5	G2
VDIN4	62	U4, V4	B7
VDIN3	61	U3, V3	B6
VDIN2	60	U2, V2	B5
VDIN1	59	U1, V1	B4
VDIN0	58	U0, V0	B3
Pixel clock	-	VCLK	VCLK
INTYPE select		INTYPE = 0	INTYPE = 1

Figure 4: AL251 Video Input

To select YUV422 or RGB565 as the input format, program the Board Configuration Register #02h, or set the hardware pin “INTYPE” (AL250 pin#11, AL251 pin#14).

3.2 AL128 Video Input Formats

Digital inputs for the AL128 can be either 24-bit RGB 888 or 16-bit RGB 565. RGB 565 can in turn be in VAFC or feature connector format. The INTYPE pins of the AL128 have to be set correctly to match the different applications.

INTYPE <1:0> Pin 156, pin 157	Digital Graphic Input Type
0 0	24-bit RGB
0 1	Reserved

1 0	Feature connector (RGB565)
1 1	VAFC (RGB565)

Figure 5: AL128B Video Input configuration table

3.2.1 24-bit RGB

The digital 24-bit RGB can be pin-to-pin wired to RED<7:0>, GREEN<7:0> and BLUE<7:0> of the AL128.

3.2.2 VAFC

The VAFC format (16-bit, RGB565, in 64k high color) carries red signals in D15~D11, green signals in D10~D5, and blue signals in D4~D0.
There are two ways to implement VAFC interface. The first way is to set INTYPE as 11 to accept VAFC format, then input the 16-bit RGB565 (64k high color) to GREEN<7:0> and BLUE<7:0> of the AL128 as follows:

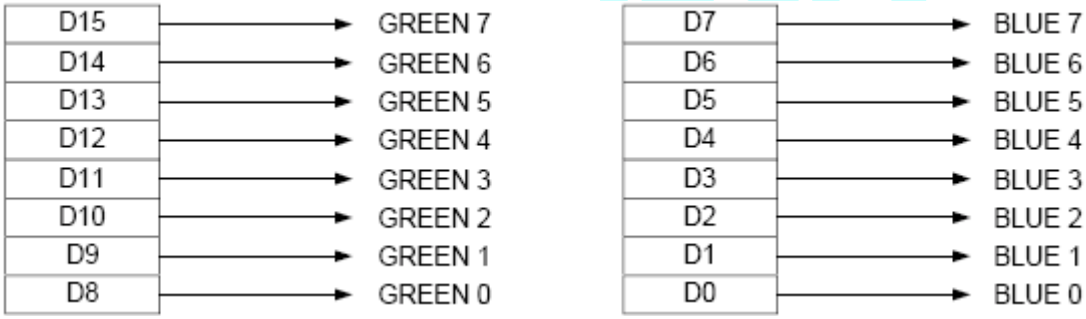


Figure 6: AL128 Video Input VAFC format

The other way is to keep INTYPE setting as 00 to accept 24-bit RGB888, but connect the inputs to the higher bits of RED<7:0>, GREEN<7:0> and BLUE<7:0> of the AL128 as follows. The unused pins can be grounded.

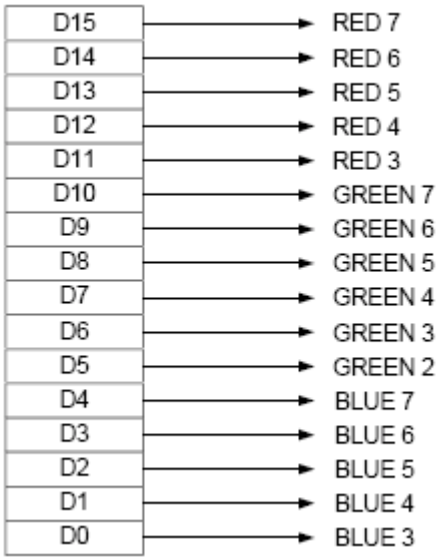


Figure 7: AL128 Video Input VAFC format

3.2.3 Feature connector

The definition of the data bits of the feature connector is the same as that of the VAFC, i.e., D15~D11 represent red signals. D10~D5 green signals, and D4~D0 blue signals. However, since the feature connector uses 8-bit interface, the two bytes of data must be received within one pixel/graphic clock (GCLK). The solution is: one byte at the rising edge and one byte at the falling edge of GCLK as follows:

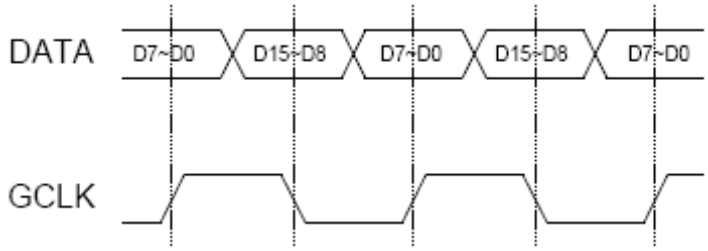


Figure 8: one byte at the rising edge and one byte at the falling edge of GCLK

The eight-bit data is wired to BLUE<7:0> of the AL128 as follows:

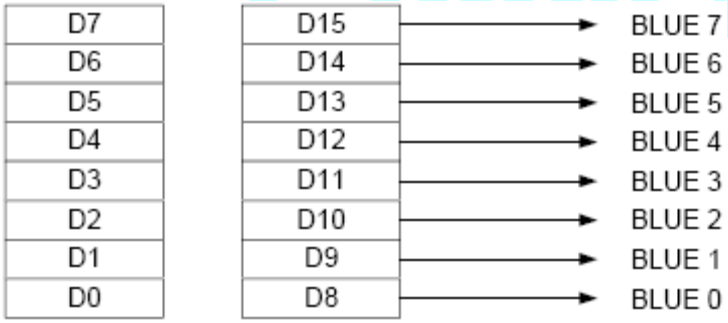


Figure 9: The eight-bit data is wired to BLUE

4 Output Formats

The AL251 provides digital output in RGB565 or YUV422 format. The pin definition and the RGB565 to 888 mapping are as follows:

Video Data Signal	AL251 Pin #	YUV 422	RGB 565
DO7	56	Y7	R7
DO6	55	Y6	R6
DO5	52	Y5	R5
DO4	51	Y4	R4
DO3	50	Y3	R3
DO2	49	Y2	G7
DO1	48	Y1	G6
DO0	47	Y0	G5
DO15	66	U7, V7	G4
DO14	65	U6, V6	G3
DO13	64	U5, V5	G2
DO12	63	U4, V4	B7
DO11	26	U3, V3	B6
DO10	25	U2, V2	B5
DO9	24	U1, V1	B4
DO8	23	U0, V0	B3
Out Format select	-	1	0

Figure 10: AL251 Video Output

5 Supported Resolutions

5.1 AL251

The resolution of the AL251 applications depends on the input video source, e.g., the digital video decoder. The typical resolution of the video decoders is as follows:

	Square pixel		CCIR 601	
	NTSC	PAL	NTSC	PAL
Pixel Total	780 x 525	944 x 625	858 x 525	864 x 625
Pixel Active	640 x 480	768 x 576	720 x 480	720 x 576

Figure 11: AL251 supporting resolutions

5.2 AL128

The resolutions that are automatically supported without any software are 640x400, 640x480 and 800x600. Other resolutions, such as 1024x768 full screen, are also supported through software programming. Scan rates up to 100 Hz are supported for 640x480 resolution, up to 85 Hz for

800x600 resolution, and up to 75 Hz for 1024x768 resolution.

6 Phase-lock-loop (GCLK recovery) circuits

Since a pixel clock (GCLK) is required for the video DSP but is not available from the VGA connector, it needs to be recovered by using a phase-lock-loop chip such as an ICS AV9173. The H-sync signal from the VGA is adjusted with its polarity so that the leading edge is always the falling edge. The adjusted signal then works as the reference sync pulse to the PLL. The AL128 receives the clock output of the PLL, generates GHSDIV signal through its divide-by-M circuitry (while M is set by the AL128 intelligently from the input sync signal detection), and sends it back to the PLL as the feedback input.

7 I²C Programming

The AL251/128 I²C programming interface is slightly different from the Philips standard. The I²C interface consists of the SCL (clock) and SDA (data) signals. Data can be written to or read from the AL251/128. For both read and write, each byte is transferred MSB first, and the SDA data bit is valid when the SCL is pulled high.

The read/write command format is as follows:

Write: <S> <Write SA> <A> <Register Index> <A> <Data> <A> <P>

Read: <S> <Read SA> <A> <Register Index> <A> <Data> <NA> <P>

Following are the details:

<**S**>:

Start signal

SCL SDA

High High

High Low

The Start signal is HIGH to LOW transition on the SDA line when SCL is HIGH.

<**WRITE SA**>:

Write Slave Address

<**READ SA**>:

Read Slave Address

<**REGISTER INDEX**>:

Value of the AL251/128 register index.

<**A**>:

Acknowledge stage

The acknowledge-related clock pulse is generated by the host (master). The host releases the SDA line (HIGH) for the AL251/128 (slave) to pull down the SDA line during the acknowledge clock pulse.

<**NA**>:

Not Acknowledge stage

The acknowledge-related clock pulse is generated by the host (master). The host releases the SDA line (HIGH) during the acknowledge clock pulse, but the AL251/128 does not pull it down during this stage.

<**DATA**>:

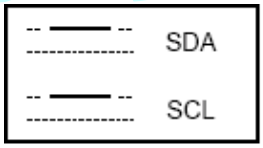
Data byte write to or read from the register index.

In read operation, the host must release the SDA line (high) before the first clock pulse is transmitted to the AL251/128.

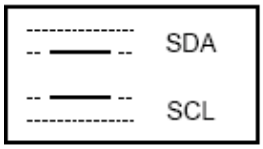
<**P**>:

Stop signal

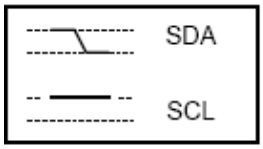
SCL SDA



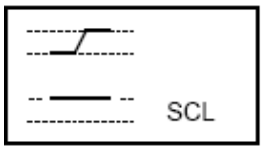
Data bit [1] or NA



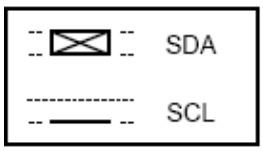
Data bit [0] or A



START bit [S]



STOP bit [P]



Not significant

High Low
High High
The Stop signal is LOW to HIGH transition on the SDA line when SCL is HIGH.

8 Using the Memory Interface

The AL128 writes processed pixel data to the FIFO memory such as AL422 with original or recovered GCLK timing, and reads the data from AL422 with TV encoding timing. The processed data is converted from RGB to temporary YUV format as follows:
Y' = (76r+150g+29b)/256
U' = (-38r-74g-112b)/256
V' = (78r-66g-12b)/256
When the AL128 and FIFO operate at high frequency, the setup time and hold time may become critical. When WCK is lagging behind the data, the GCLK can also be used as write clock since GCLK may be a few nanoseconds ahead of WCK.

9 Board Design and Layout Considerations

9.1 Analog Signal Traces

- From AV Jacks to AI0, AI1, AI2 or AI3, These critical analog paths should be 8~12 mil of width using point-to-point routing without vias.
- Digital signals such as clocks and data signals should be kept as far away from the analog signal traces as possible.
- Putting the 10uF and 0.1uF ceramic-chip capacitors that belong to VBG, VREFP, VREFN, and VCM close to AL242.
- Putting the DC restore circuit of 50Ohm resister, 47pF and 220nF capacitors that belong to each analog input close to AL242.

9.2 Grounding

- Use a 5-mil separation material between power and ground planes if a four-layer board is used.
- The ground plane should be solid, not cross-hatched.
- Separate the analog and digital ground planes and connect them at a single point through a low resistance ferrite bead.
- All the connections to the ground plane should have very short leads
- Analog and digital circuits are separated within the AL251 and AL128 chip. To minimize system noise and prevent digital system noise from entering the analog portion, a common ground plane for all devices, including the AL251 and AL128, is recommended.

9.3 Power Planes

- The analog power plane should be connected to the digital power plane at a single point through a low resistance ferrite bead. (If they have the same voltages.)
- Use 0.1μF ceramic-chip capacitors for each power supply pin with no more than ½” trace length.
- To minimize low frequency power ripple, use a 22μF capacitor between each power plane and ground.

9.4 Digital Signal Traces

- Keep digital signal traces as far apart from analog signal traces as possible.
- Critical digital signal traces such as clocks should be 8~12 mil of width using point-to-point routing without vias.

- Jitter and noise on the clock can significantly degrade the video performance. Keep the clock paths as short as possible.

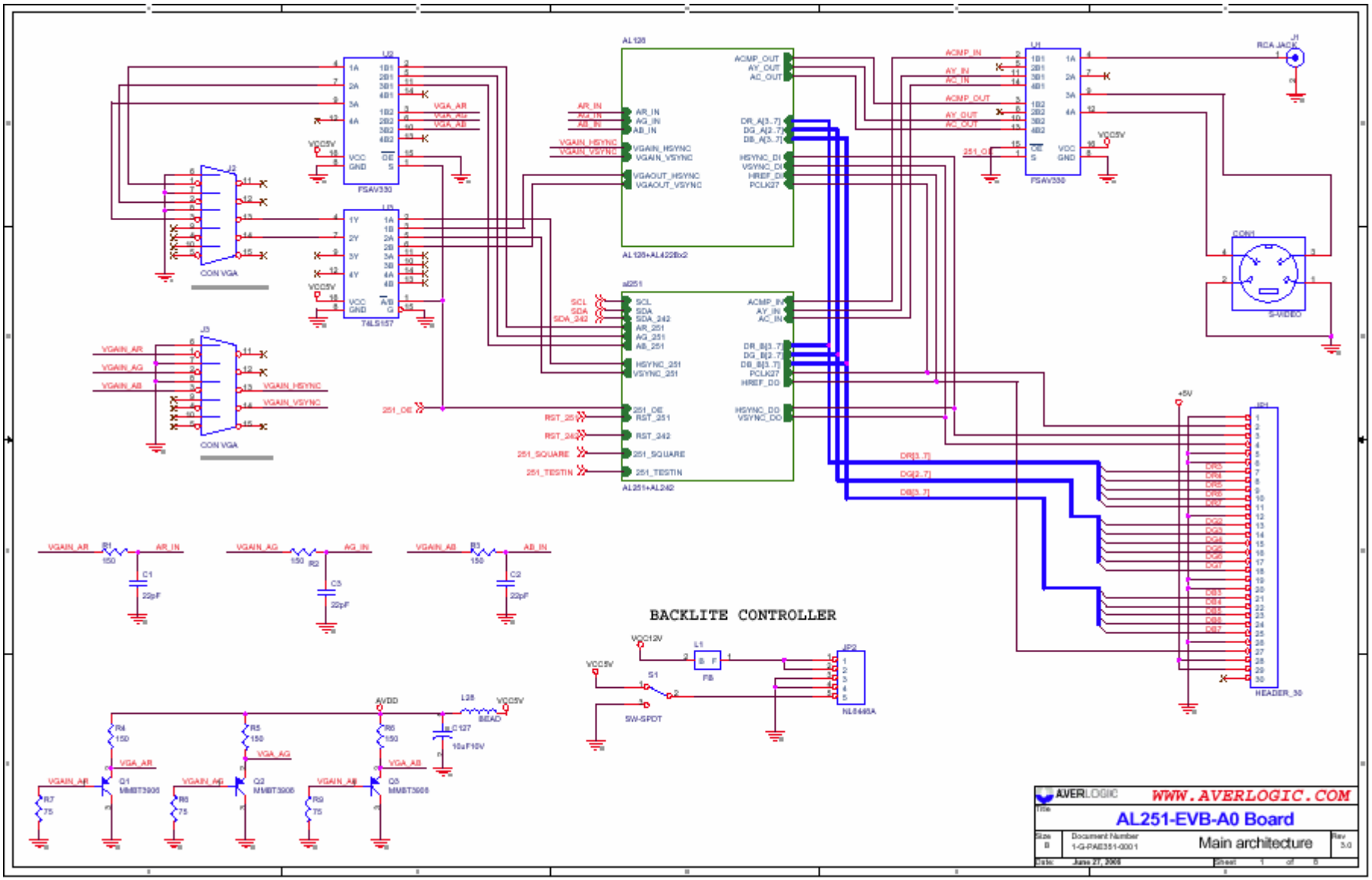
9.5 Analog Signal Interconnect

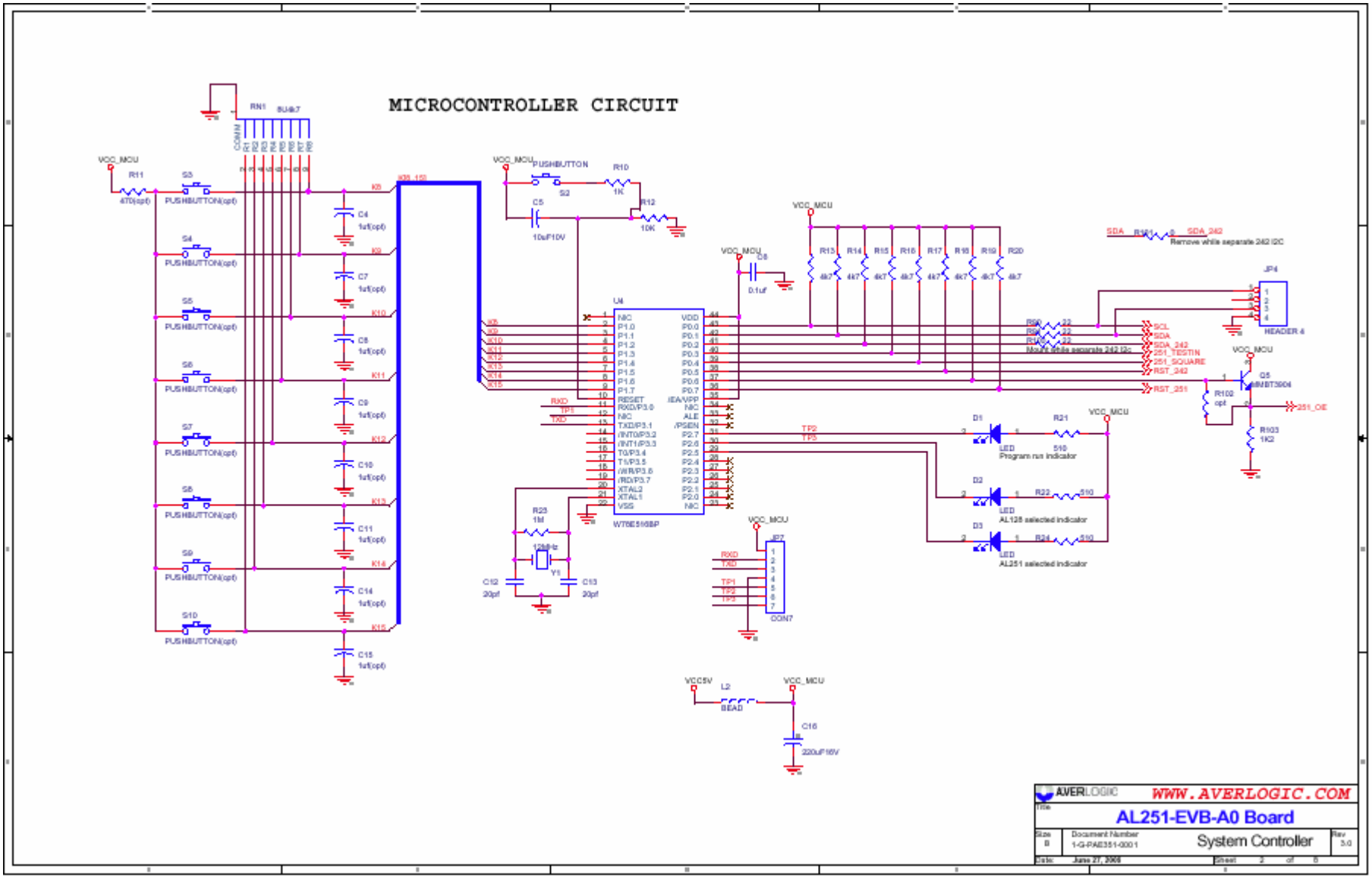
- The AL251 should be located closely to the output connectors to minimize noise and reflections. Keep the critical analog traces as short and wide as possible.
- Digital signals, especially pixel clocks and data signals should not overlap any of the analog signal circuitry and should be kept as far apart as possible.
- The AL251 and the decoder IC should have no inputs left floating. Each of the unused analog input pins should be connected to GND.

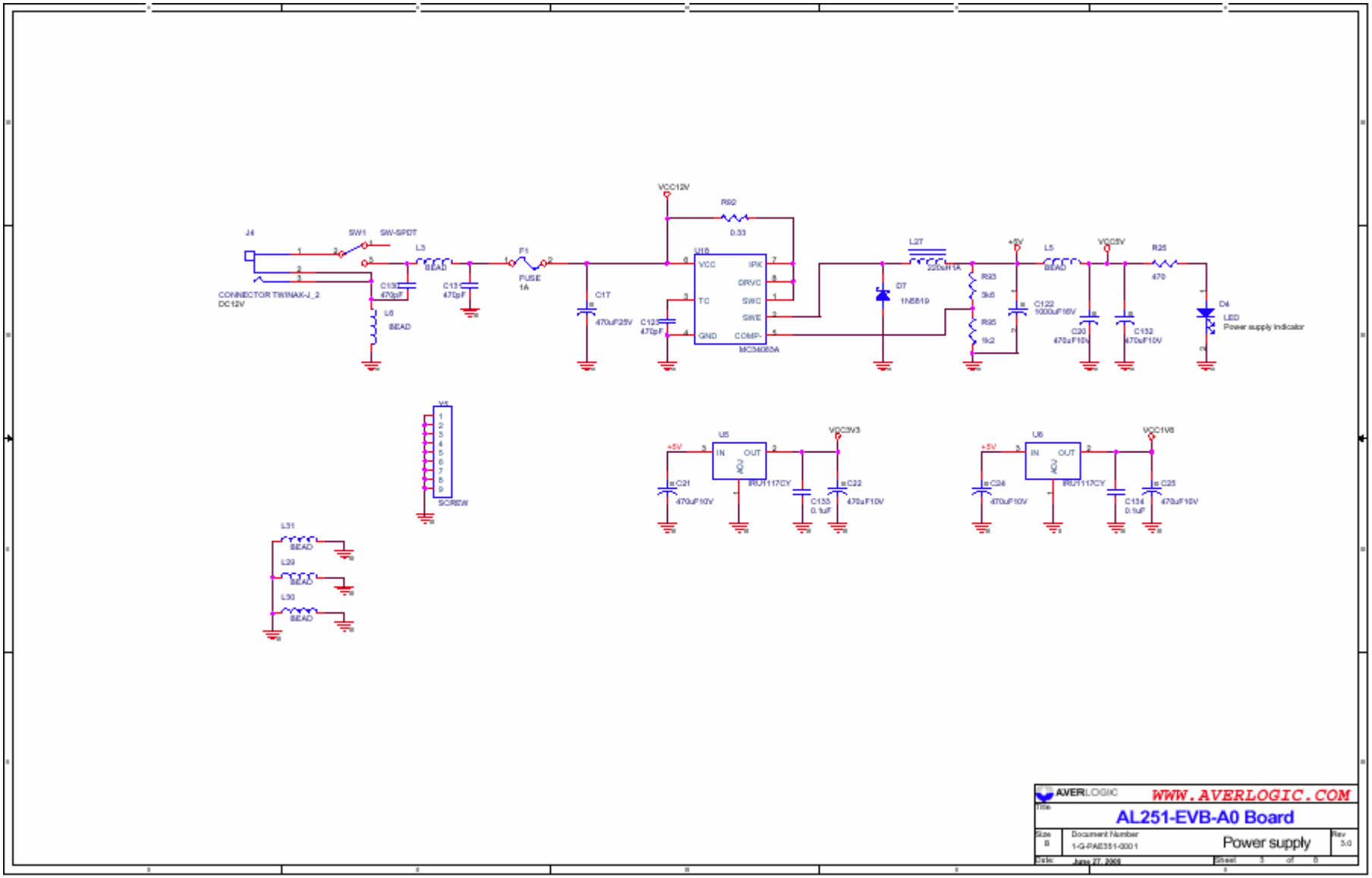
10 More Information

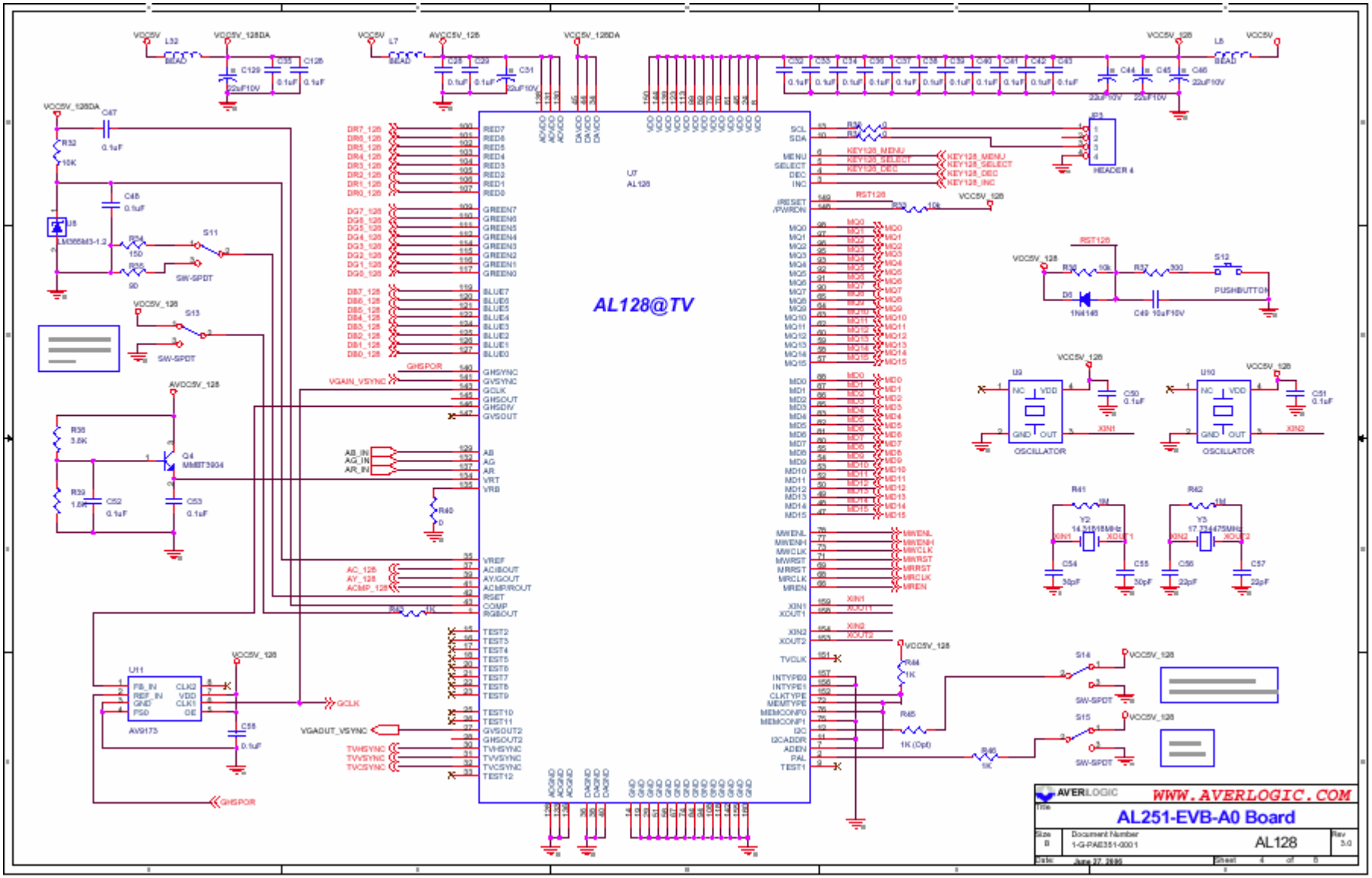
The reference design circuit is attached in the end of this application note. The following information is also available upon request, please contact us, your local authorized representatives or distributors.

11 APPENDIX-2: AL251-EVB-A0 Reference Schematics





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U7
AL128
AV9173
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OSCILLATOR
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SW-SPDT
PUSHBUTTON
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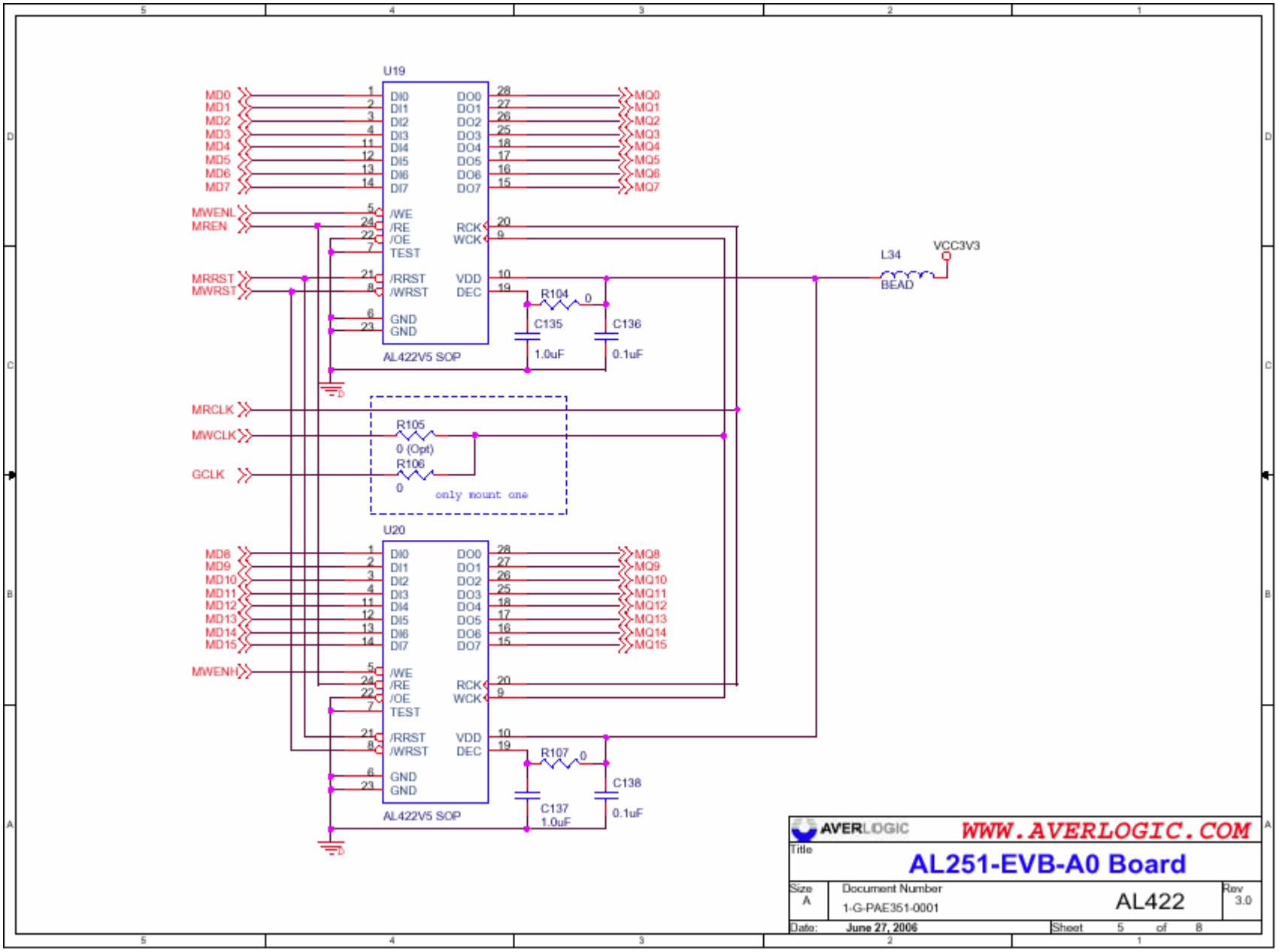

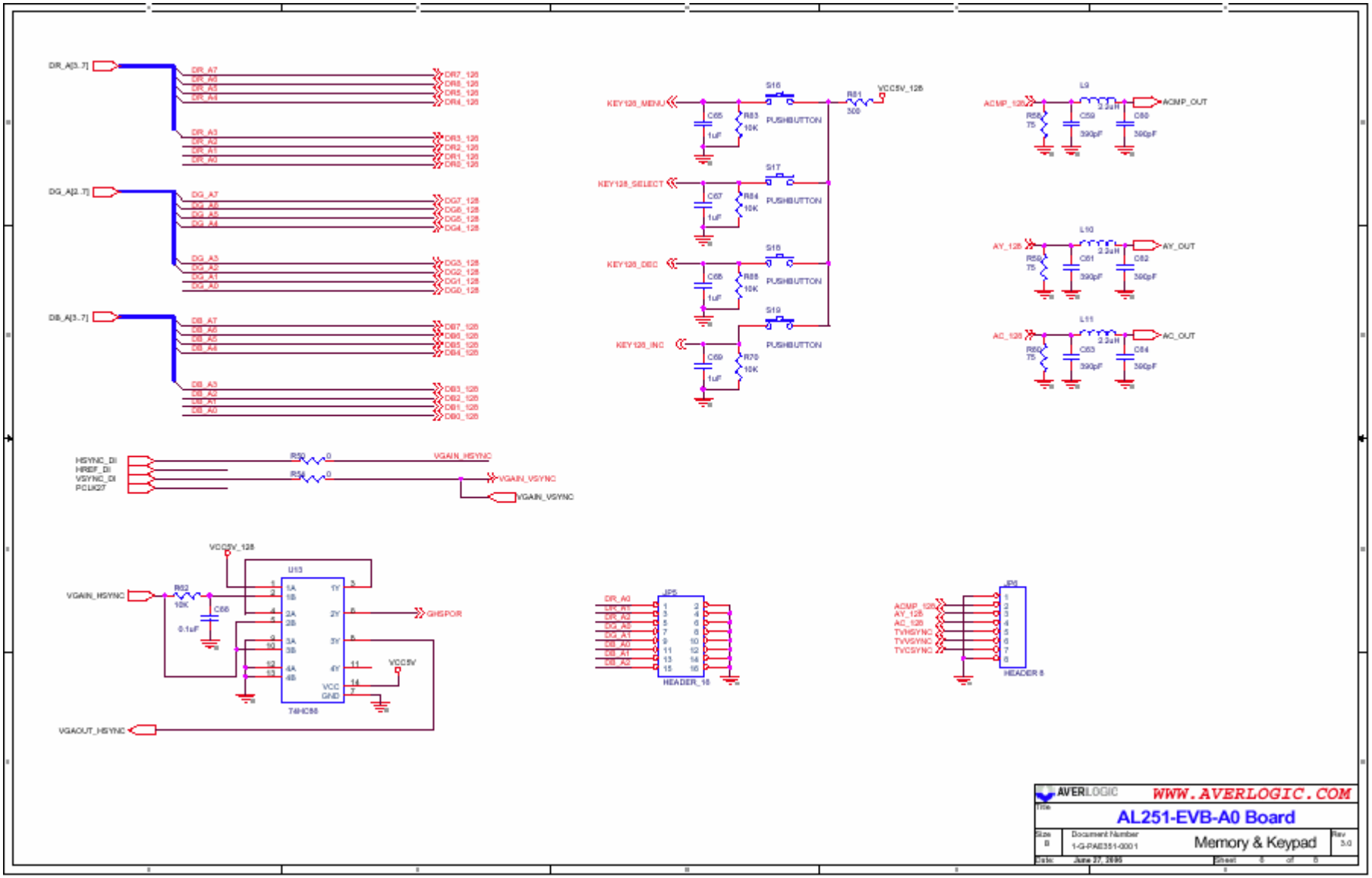

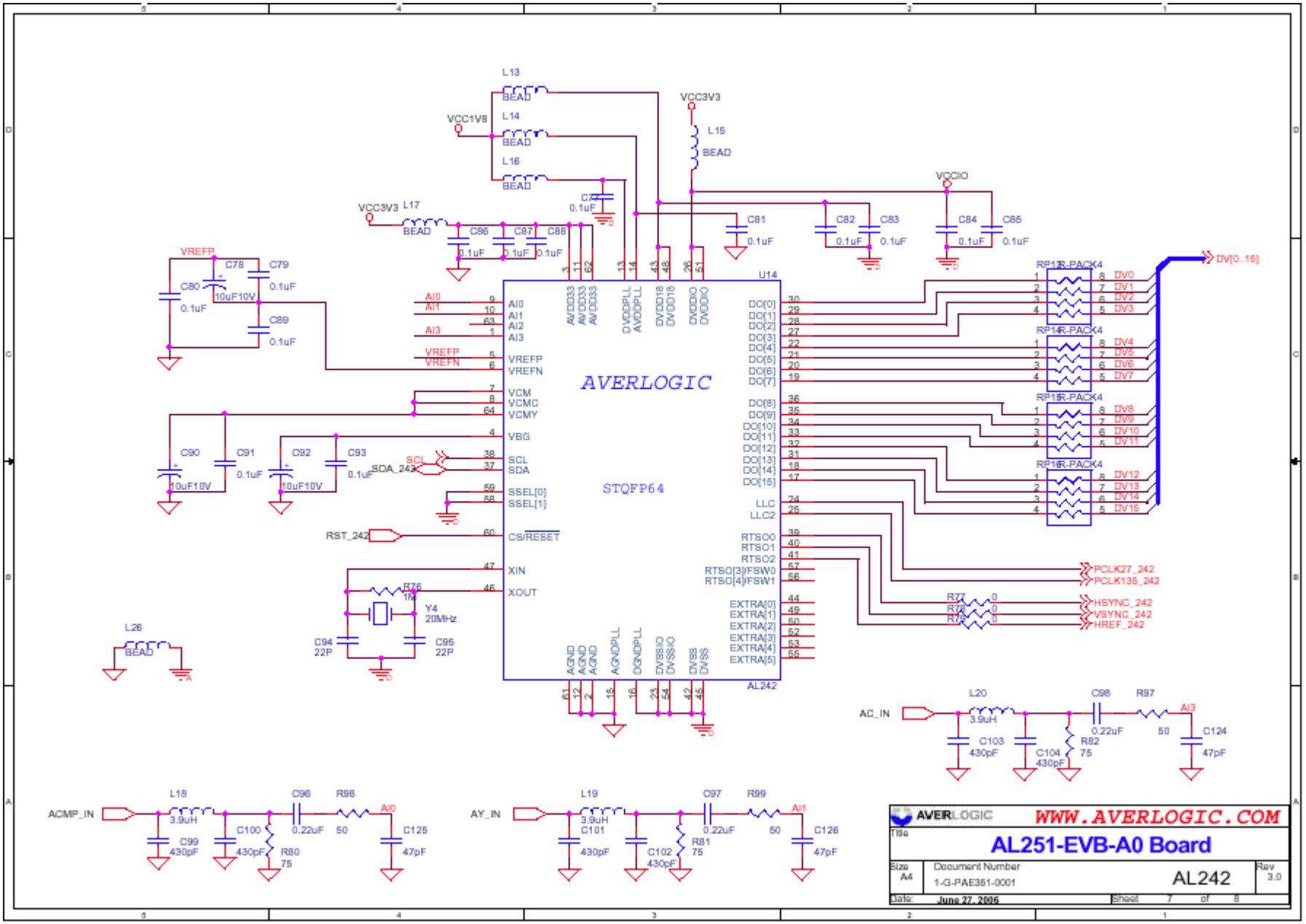

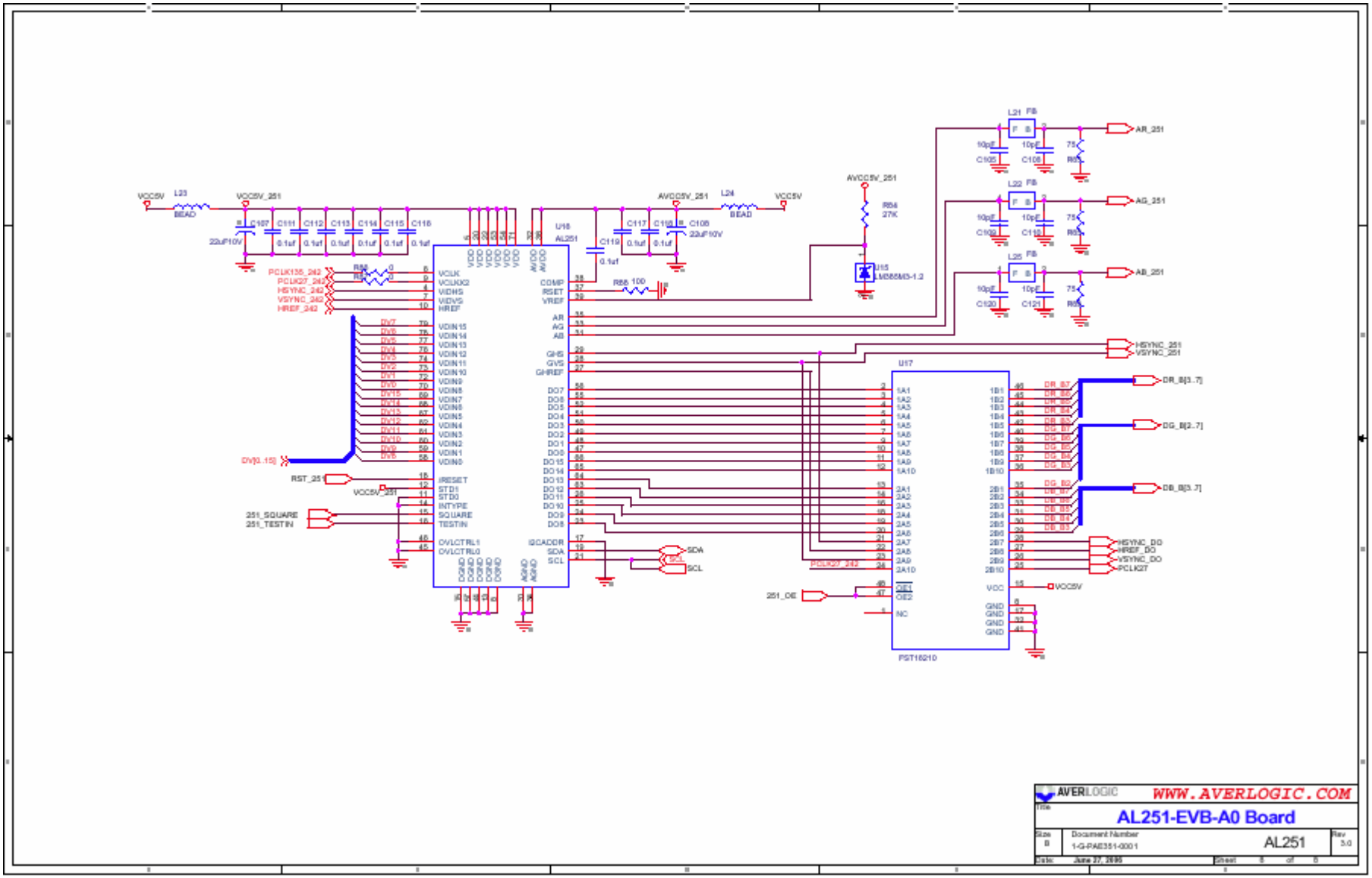
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PST16210
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HSYNC_251
VSYNC_251
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VSYNC_DO
PCLK27
SDA
SCL
RST_25
251_SQUARE
251_TESTIN
251_OE
VCC5V
AVCC5V_251

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