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(54) **DISPLAY FOR A COMPUTER.**

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Description

The present invention relates to computers and more particularly to coloured displays for computers.

Coloured displays for computers are already well known but most conventional displays require large amounts of memory for producing high resolution graphics in colour as well as complex circuitry.

GB 2044052 discloses an apparatus for producing a coloured display from a computer, comprising a memory for storing digital words corresponding to a pattern to be displayed, and a smaller number of digital words corresponding to the colour of the pattern to be displayed. Each colour word is associated with a number of pattern words. The words are read out of memory and digital colour signals are produced in response to the pattern and colour words.

The present invention provides an apparatus for producing a coloured display from a computer as defined in the attached claims.

Features and advantages of the present invention will become apparent from the following description given by way of example when taken in conjunction with the accompanying drawings, in which:—

Figure 1 shows a block circuit diagram of part of the circuit for generating high resolution graphics in colour;

Figure 2 shows a circuit for generating one of the colour difference signals for the PAL system of television;

Figure 3 shows a circuit for generating the other colour difference signal for the PAL system of television;

Figure 4 shows a circuit for generating the luminance signal for the PAL system of television; and

Figure 5 shows a detailed circuit diagram of the arrangement shown in Figure 1 and for producing the signals used for the circuits shown in Figures 2, 3 and 4.

Before describing the invention, it is considered helpful if a general discussion of the graphics is given first. Conventionally a VDU read out for a computer consists of a "page" of characters on the screen of the VDU arranged in rows and columns. For the sake of the present discussion it is assumed that there are 24 rows with 32 character locations in each row of the display. It is also assumed that the size of each character position is such that 8 raster scan lines are required to fully display one row of the display. With this arrangement, it is apparent that not all the active area of the television screen is utilised by the display but this is not considered to be a disadvantage due to the fact that the display can be generated for either a 525 line television system or a 625 line television system.

The character locations of the display can be used to display either alpha-numeric symbols or graphical symbols but it will be appreciated that when displaying graphical symbols, the display will be somewhat crude due to the small number of character locations. It has already been proposed to sub-divide the character locations for graphics display using what are termed "pixels" and it is this latter concept which we are using. In our case, we envisage notionally dividing up the display area into a matrix of pixels of 192 rows each containing 256 pixels.

When displaying a matrix of pixels in black and white, the amount of memory required is manageable but as soon as one wishes to display in colour, the amount of memory required increases considerably if each pixel is to have it own individual colour.

We have now produced an arrangement whereby the background colours are treated in the "old" manner as if the display were still displaying character positions whereas the foreground colour is displayed as a pixel plane display with a consequent considerable saving in the amount of memory required. In other words each character location requires 8 bytes of data to define the dot pattern i.e. the pixel pattern in the character location but only 1 byte of data, the attribute byte, for the colour of the character location. Each attribute byte comprises a number of bits representing the foreground colour, a number of bits representing the background colour and preferably a bit to indicate whether or not to cause the character location to flash and also preferably a further bit to allow two different levels of illumination to cause particular desired areas to be highlighted. The number of bits required for the colour information is chosen having regard to the size of the byte and the number of colours which it is wished to use. In the present case, eight colours are used which means that 3 bits are required for background colour and 3 bits for foreground colour giving an 8 bit attribute byte. Thus, a high resolution graphics display can be produced in colour using a one memory device, namely a random access memory of the dynamic type. The size of the memory device is a function of the number of pixels and also the number of attribute bytes. With our system of 192×256 pixels and 768 character locations, the memory device has to be capable of storing approximately 6k bytes of data for the 192×256 pixel pattern plus approximately $\frac{3}{4}$k of data for the attribute bytes for the 768 character locations.

As mentioned above, each character location consists of eight pixels horizontally by eight rows i.e. TV raster scan lines vertically. In order to generate the raster scan TV picture, the memory device has to be accessed sequentially in a cycle that repeats every TV field. For every eight pixels generated, the computer needs two bytes of data from memory, a pixel pattern byte and an attribute byte. These two bytes are loaded into respective intermediate registers from which they then are loaded into further registers. The six least significant bits of the attribute byte represent the foreground and background colours. A data selector is controlled by the pixel

pattern bytes shifted out of their register to select foreground or background colour for each pixel and fed to a colour generator circuit for generating a 3 bit (R.G.B) signal for each pixel.

The operation of the memory and registers will now be described in more detail with reference to Figure 1. Eight bit data words (bytes) are fed from memory (not shown) to eight input pins DØ to D7. The eight bits of each word are fed in parallel to the inputs of an intermediate pixel pattern latch 10 and an attribute latch 11. The latch 10 or the latch 11 is gated by the processor depending on whether the data to be loaded into the latch is pixel pattern data or colour (attribute) data. For each raster scan line, the memory is addressed to sequentially recover the 32 pixel pattern bytes for the 256 pixels for that line. With each of these bytes, a further portion of memory is addressed in order to recover the attribute byte for eight pixels associated therewith.

Since each of the latches 10 and 11 are connected in parallel to the pins D0 to D7 and are clocked by different phases of a clock signal, it is necessary to address the memory device to deliver alternately the pixel pattern byte and associated colour attribute byte.

The data in the latch 10 is then transferred to a further latch 15. The bits of data held in the latch 15 are shifted out serially. Each bit represents a pixel and the logical level of each bit determines whether it is a foreground or a background pixel. Each bit as it is shifted out is used to gate a 3-channel 2 line to 1 line selector 16 via a logic circuit 17 which will be described in more detail later. The result is a 3-bit R, G, or B signal.

Attribute data held in latch 11 is likewise transferred to a further latch 20. It will be recalled that 6 bits of the 8 bit data word represent foreground and background colours. These six bits are fed to the data selector 16. The remaining two bits are control bits one for indicating the level of brightness of the display for that pixel, this being indicated by the output labelled HL and the other for indicating whether or not flashing of the pixel is required, this being indicated by the output labelled FL. Flashing, in this case, is achieved by causing the pixel in question to alternately display the foreground and background colour at a rate determined by a clock signal T. Thus, the logic circuit 17 contains an inverter 17a for inverting the signal on the output FL and feeding the inverted signal as an input an OR gate 17b to whose input clock signal T is applied. The output of the gate 17b is fed as one input to an EX-OR gate 17c whose other input is the data bit indicating a foreground pixel.

In operation if a data bit representing a foreground pixel is shifted out of the latch 15 to one input to the EX-OR gate 17c, the data selector 16 is conditioned to cause the 3 bits of attribute data indicative of a foreground colour to be fed to the Blue, Red and Green outputs of the selector. If flashing is required, a signal is cyclically applied to the other input of the EX-OR gate 17c to cause its output to alternate which in turn causes the output from the data selector to alternate the foreground and background colours.

It will be noted that a further latch 22 and data selector 23 are present. These are used so that the colour of the picture area around the pixel display area on the television screen can be defined to have a different colour to that of the background of the pixel display area.

This process is repeated along a raster line with 32 pixel pattern bytes being successively fed to the latch 10 and the 32 associated attribute bytes being successively fed to the latch 11. For the next line, a fresh set of 32 pixel pattern bytes are transferred successively from memory to the latch 10 but the associated attribute bytes are the same as the previous line. This process is repeated line by line until 8 lines have been displayed. Thereafter a fresh set of attribute bytes are used for the next 8 lines.

Although the output of the data selector 16 is an indication of the colour required, it is not in a form which can be utilised by the colour circuits of a conventional television receiver and so further processing of the R.G.B output from the data selector 16 is required. A further aspect of the present invention lies in the circuitry used to process the R,G,B signals into the more conventional Y,U,V signals.

Attention is directed now to Figure 2 which shows a circuit for deriving the U signal for a colour television receiver. The digital R,G,B outputs from the data selector 16 are combined with sync, blank and burst signals to provide correct phase digital signals in a digital to analogue converter circuit which is shown in Figure 2. It will be seen that the R,G,B signals are now $\overline{\text{Blue''}}$ $\overline{\text{Green''}}$ and $\overline{\text{Red''}}$ and are used to gate a respective transistor switch 31, 32, 33 to cause varying amounts of base bias to be applied to an output transistor 34. The $\overline{\text{Burst}}$ signal is also used to gate a transistor 36 which also varies the amount of base bias on transistor 34. This is achieved by all the $\overline{\text{Blue''}}$, $\overline{\text{Green''}}$, $\overline{\text{Red''}}$ and $\overline{\text{Burst}}$ circuits being connected between the emitter of a control transistor 35 and ground thus varying the current through the control transistor when it is switched on as a function of whether one or more of the switches controlled by the $\overline{\text{Blue''}}$, $\overline{\text{Green''}}$, $\overline{\text{Red''}}$ and $\overline{\text{Burst}}$ is operated.

Figure 3 shows a circuit similar to Figure 2 but for the V signal. Equivalent parts of Figure 2 are increased by ten in Figure 3 and further description will be omitted except to say that in this case the R,G,B signals are combined with the sync, blank and burst signals to form Red*, $\overline{\text{Green*}}$, $\overline{\text{Blue*}}$, $\overline{\text{Burst*}}$ and Burst* input signals to transistors 43, 42, 41, 46 and 48 respectively.

Figure 4 shows the luminance digital to analogue converter circuit which in addition to the Red', Green', Blue' and $\overline{\text{Sync}}$ signals derived from the output of the data selector 16 has a further input $\overline{\text{HL}}$ which is derived from the high-light data bit in the attribute bytes.

As with the circuits in Figures 2 and 3, Red', Green' and Blue' signals are used to gate tran-

sistors 53, 52, 51 respectively which are in the emitter circuit of a control transistor 55. The $\overline{HL}$ signal is used to gate a transistor 56 which affects the base current to the control transistor 55. The $\overline{sync}$ signal gates a further transistor 57 which is used to directly control the base bias of the output transistor 54.

Detailed description of the circuit shown in Figures 2, 3 and 4 is omitted since resistance values are given on the drawings and it is considered that in view of this, the operation is apparent to one skilled in the art.

The circuits shown in Figures 2, 3 and 4 have been designed for their simplicity and also so that they can be incorporated as peripheral circuits of an uncommitted logic array (ULA) which can be used to provide the remainder of the colour and pixel matrix display circuit.

For completeness, Figure 5 which is made up of Figures 5A, 5B, 5C and 5D shows a detailed circuit diagram showing in detail the construction of the blocks shown in Figure 1 as well as the circuits for producing the correct phase R,G,B signals used in Figures 2, 3 and 4. Where appropriate the blocks are shown in Figure 5 in broken lines and given the same reference numeral as in Figure 1. The circuits shown in Figures 2, 3 and 4 are contained in the block 60 in Figure 5D.

Claims

1. Apparatus for producing a coloured display from a computer, comprising memory means for storing a multiplicity of first digital words each constituted by a plurality of binary digits and representing a pattern to be displayed, and a smaller number of second digital words each constituted by a plurality of binary digits and representing the colour of the pattern to be displayed, each of said second digital words being associated with a plurality of the first digital words, means for reading said first and second words out of the memory means, and digital colour signal generating means (16) responsive to said first and second digital words for producing digital colour signals for a portion of a line of a video raster scan characterised in that the memory means is a dynamic random access memory device having first and second locations for storing said first and second words and having a number of outputs (D0—D7) equal in number to the number of digits in a digital word, two latch arrangements (10, 15, and 11, 12) each connected to the outputs (D0—D7) of the memory device and each clocked to receive a respective one of said first and second digital words, and means for successively addressing the first and second locations whereby to output from the device successively first and second digital words to the latch arrangements.

2. Apparatus according to claim 1, wherein one of the two latch arrangements (10, 15) includes a first latch (15) for receiving a first digital word and for outputting the binary digits thereof in a serial manner.

3. Apparatus according to claim 2, wherein each of the second digital words includes data representing both foreground and background colour information, and the colour signal generating means (16) includes a 2 channel into 1 data selector (16) responsive to the logical level of each of the binary digits output from the first latch (15) whereby the colour information representing the foreground or the background information is generated.

4. Apparatus according to claim 2 or 3, wherein said one of the two latch arrangements (10, 15) includes a further latch (10) between the outputs (D0—D7) of the memory device and the first latch (15).

5. Apparatus according to claim 4, wherein the other of the two latching arrangements (11, 20) comprises a series of two latches connected between the outputs of the memory device and the digital signal generating means (16).

6. Apparatus according to any one of the preceeding claims and comprising digital to analogue conversion circuitry for producing analogue colour signals from the digital signals output from the digital colour signal generating means.

7. Apparatus according to claim 6, wherein the conversion circuitry comprises three digital to analogue conversion circuits, one (Fig. 2) for generating an analogue signal representing a U signal, one (Fig. 3) for generating an analogue signal representing a V signal, and one (Fig. 4) for generating an analogue signal representing a Y signal.

8. Apparatus according to claim 6, wherein each of the digital to analogue conversion circuits comprises an output transistor (34, 44, 54) whose base bias is controllable by a control transistor (35, 45, 55) in whose emitter circuit are connected further switching devices (31—36, 36; 41—43, 46, 48; 51—53, 56, 57) responsive to the signal derived from the digital colour signal generating means (16).

Patentansprüche

1. Vorrichtung zum Erzeugen einer farbigen Computer-Anzeige mit einem Speicher zum Speichern einer Vielzahl von ersten digitalen Worten, die jeweils aus einer Vielzahl von binären Einheiten bestehen und eine anzuzeigende Struktur repräsentieren und einer geringeren Anzahl von zweiten digitalen Worten, die jeweils aus einer Vielzahl von binären Einheiten bestehen und die Farbe der anzuzeigenden Struktur repräsentieren, wobei jedes der genannten zweiten digitalen Worte einer Vielzahl von ersten digitalen Worten zugeordnet ist, mit Einrichtungen zum Lesen der ersten und zweiten Worte aus dem Speicher, und einer Einrichtung (16) zum Erzeugen digitaler Farbsignale, welche auf die genannten ersten und zweiten digitalen Worte anspricht, um digitale Farbsignale für einen Abschnitt einer Linie einer Video-Rasterabtastung zu erzeugen, dadurch gekennzeichnet, daß als Speicher ein dynami-

scher Speicher mit wahlfreiem Zugriff (DRAM) vorgesehen ist, der erste und zweite Plätze zum Speichern der genannten ersten bzw. zweiten Worte aufweist sowie eine Anzahl von Ausgängen (D0—D7), deren Anzahl der Anzahl der binären Einheiten eines digitalen Wortes entspricht, zwei Haltekreise (10, 15 und 11, 12), die jeweils mit den Ausgängen (D0—D7) des Speichers verbunden sind und die jeweils getaktet werden, um das Zugeordnete der ersten und zweiten digitalen Worte zu empfangen, und daß eine Einrichtung zum sukzessiven Adressieren der ersten und zweiten Speicherplätze vorgesehen ist, wodurch von der Einrichtung nacheinander erste und zweite digitale Worte an die Haltekreise abgegeben werden.

2. Vorrichtung gemäß Anspruch 1, wobei einer der zwei Haltekreise (10, 15) einen ersten Haltekreis (15) aufweist zum Empfangen eines ersten digitalen Wortes und zum seriellen Ausgeben von dessen binären Einheiten.

3. Vorrichtung nach Anspruch 2, wobei jedes der zweiten digitalen Worte Daten enthält, die sowohl die Vordergrund- als auch die Hintergrund-Farbinformation repräsentieren, wobei die Farbsignal-Erzeugungseinrichtung (16) einen Daten-Selektor (16) aufweist, der zwei Kanäle in einen umsetzt und auf den logischen Pegel jedes der vom ersten Haltekreis (15) abgegebenen binären Einheiten anspricht, wodurch die dem Vordergrund oder dem Hintergrund entsprechende Farb-Information erzeugt wird.

4. Vorrichtung nach einem der Ansprüche 2 oder 3, wobei der genannte eine der beiden Haltekreise (10, 15) einen weiteren Haltekreis (10) zwischen den Ausgängen (D0—D7) des Speichers und dem ersten Haltekreis (55) aufweist.

5. Vorrichtung nach Anspruch 4, wobei der andere der beiden Haltekreise (11, 20) eine Reihenschaltung von Haltekreisen aufweist, die zwischen den Ausgängen des Speichers und der Einrichtung (16) zum Erzeugen eines digitalen Signales angeordnet sind.

6. Vorrichtung nach einem der vorhergehenden Ansprüche mit einem Digital/Analog-Wandler zum Erzeugen analoger Farbsignale aus den digitalen Signalen, die vom digitalen Farbsignal-Generator (16) abgegeben werden.

7. Vorrichtung nach Anspruch 6, wobei der Wandler drei Digital/Analog-Konverter aufweist, wovon einer (Fig. 2) dazu dient, ein Analogsignal zu erzeugen, welches ein U-Signal repräsentiert, während ein anderer (Fig. 3) dazu dient, ein Analogsignal zu erzeugen, welches ein V-Signal repräsentiert und während ein anderer (Fig. 4) dazu dient, ein Analogsignal zu erzeugen, welches einem Y-Signal entspricht.

8. Vorrichtung nach Anspruch 6, wobei jeder der Digital/Analog-Konverter einen Ausgangstransistor (34, 44, 54) aufweist, dessen Basis-Vorspannung mittels eines Steuertransistors (35, 45, 55) steuerbar ist, in dessen Emitter-Schaltkreis weitere Schalteinrichtungen (31 bis 36, 36; 41 bis 43; 46, 48; 51 bis 53, 56, 57) geschaltet sind, welche auf die Signale ansprechen, die vom digitalen Farbsignal-Erzeuger (16) abgeleitet werden.

Revendications

1. Appareil pour la production d'un affichage en couleurs à partir d'un ordinateur, comprenant un moyen de mémorisation propre à mémoriser une série de premiers mots numériques constitués chacun par plusieurs chiffres binaires et représentant une configuration à afficher, et un nombre plus petit de seconds mots numériques constitués chacun par plusieurs chiffres binaires et représentant la couleur de la configuration à afficher, chacun desdits seconds mots numériques étant associé à plusieurs d'entre les premiers mots numériques, un moyen de lecture desdits premiers et seconds mots dans le moyen de mémorisation, et un moyen générateur de signaux de couleur numériques (16) propre à réagir auxdits premiers et seconds mots numériques pour fournir des signaux de couleur numériques pour une portion d'une ligne de balayage de trame vidéo, caractérisé en ce que le moyen de mémorisation est un dispositif de mémoire dynamique à accès direct comportant de premiers et de seconds emplacements pour la mémorisation desdits premiers et seconds mots et comportant un nombre de sorties (D0 à D7) égal au nombre de chiffres d'un mot numérique, deux montages à bascules (10, 15 et 11, 12) connectés chacun aux sorties (D0 à D7) du dispositif de mémoire et cadencés chacun de manière à recevoir l'un respectif desdits premiers et seconds mots numériques, et un moyen propre à adresser successivement les premiers et seconds emplacements de sorte que le dispositif délivre successivement des premiers et seconds mots numériques aux montages à bascules.

2. Appareil selon la revendication 1, dans lequel l'un des deux montages à bascules (10, 15) comporte une première bascule (15) pour recevoir un premier mot numérique et pour en sortir en série les chiffres binaires.

3. Appareil selon la revendication 2, dans lequel chacun des seconds mots numériques contient des données représentant de l'information de couleur d'avant-plan et de couleur de fond, et le moyen générateur de signaux de couleur (16) comporte un sélecteur de données des 2 canaux en 1 (16) réagissant au niveau logique de chacun des chiffres binaires de sortie de la première bascule (15) en générant ainsi l'information de couleur représentant l'information d'avant-plan ou de fond.

4. Appareil selon la revendication 2 ou 3, dans lequel ledit montage à bascule (10, 15) comporte une bascule additionnelle (10) entre les sorties (D0 à D7) du dispositif de mémoire et la première bascule (15).

5. Appareil selon la revendication 4, dans lequel l'autre montage à bascules (11, 20) comprend une série de deux bascules connectées entre les sorties du dispositif de mémoire et le moyen générateur de signaux numériques (16).

6. Appareil selon l'une quelconque des revendications précédentes et comprenant des circuits de conversion numérique-analogique pour la production de signaux de couleur analogiques à partir des signaux numériques délivrés par le moyen générateur de signaux de couleur numériques.

7. Appareil selon la revendication 6, dans lequel les circuits de conversion comprennent trois circuits de conversion numérique-analogique, l'un (Fig. 2) pour générer un signal analogique représentant un signal U, l'un (Fig. 3) pour générer un signal analogique représentant un signal V et l'un (Fig. 4) pour générer un signal analogique représentant un signal Y.

8. Appareil selon la revendication 6, dans lequel chacun des circuits de conversion numérique-analogique comprend un transistor de sortie (34, 44, 54) dont la polarisation de base est réglable par un transistor de commande (35, 45, 55) dans le circuit d'émetteur duquel sont connectés des dispositifs de commutation additionnels (31 à 36, 36; 41 à 43, 46, 48; 51 à 53, 56, 57) sensibles aux signaux provenant du moyen générateur de signaux de couleur numériques (16).

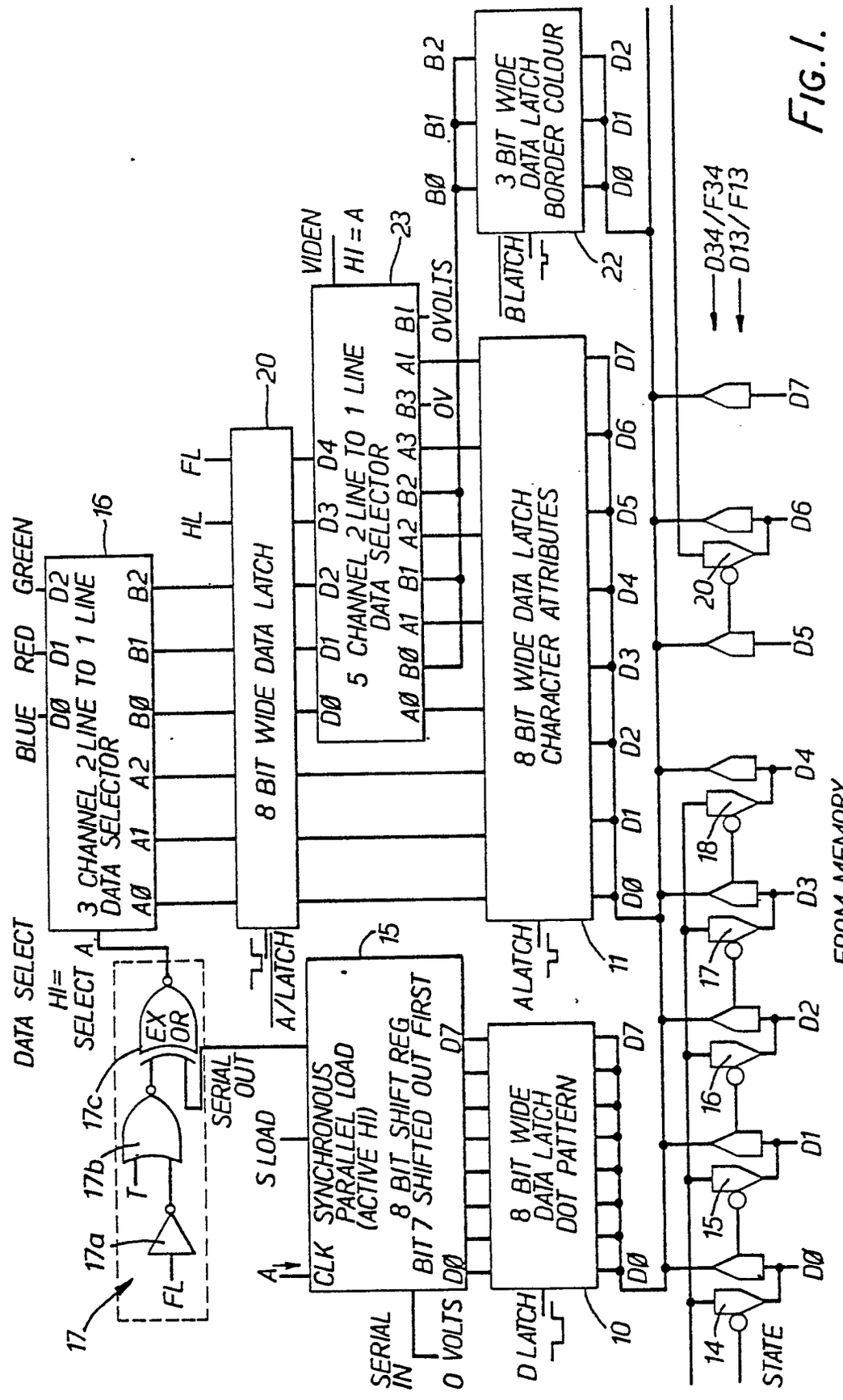
DATA SELECT
HI= SELECT A
BLUE
RED
GREEN
3 CHANNEL 2 LINE TO 1 LINE DATA SELECTOR
16
8 BIT WIDE DATA LATCH
20
HL
FL
A/LATCH
VIDEN
HI = A
5 CHANNEL 2 LINE TO 1 LINE DATA SELECTOR
23
OVOLTS
3 BIT WIDE DATA LATCH BORDER COLOUR
B LATCH
22
8 BIT WIDE DATA LATCH CHARACTER ATTRIBUTES
A LATCH
11
SERIAL OUT
S LOAD
SYNCHRONOUS PARALLEL LOAD (ACTIVE HI)
8 BIT SHIFT REG
BIT 7 SHIFTED OUT FIRST
15
SERIAL IN
0 VOLTS
8 BIT WIDE DATA LATCH DOT PATTERN
D LATCH
10
EX OR
17
17a
17b
17c
FL
D34/F34
D13/F13
FROM MEMORY
STATE
14

FIG. 1.

U SIGNAL

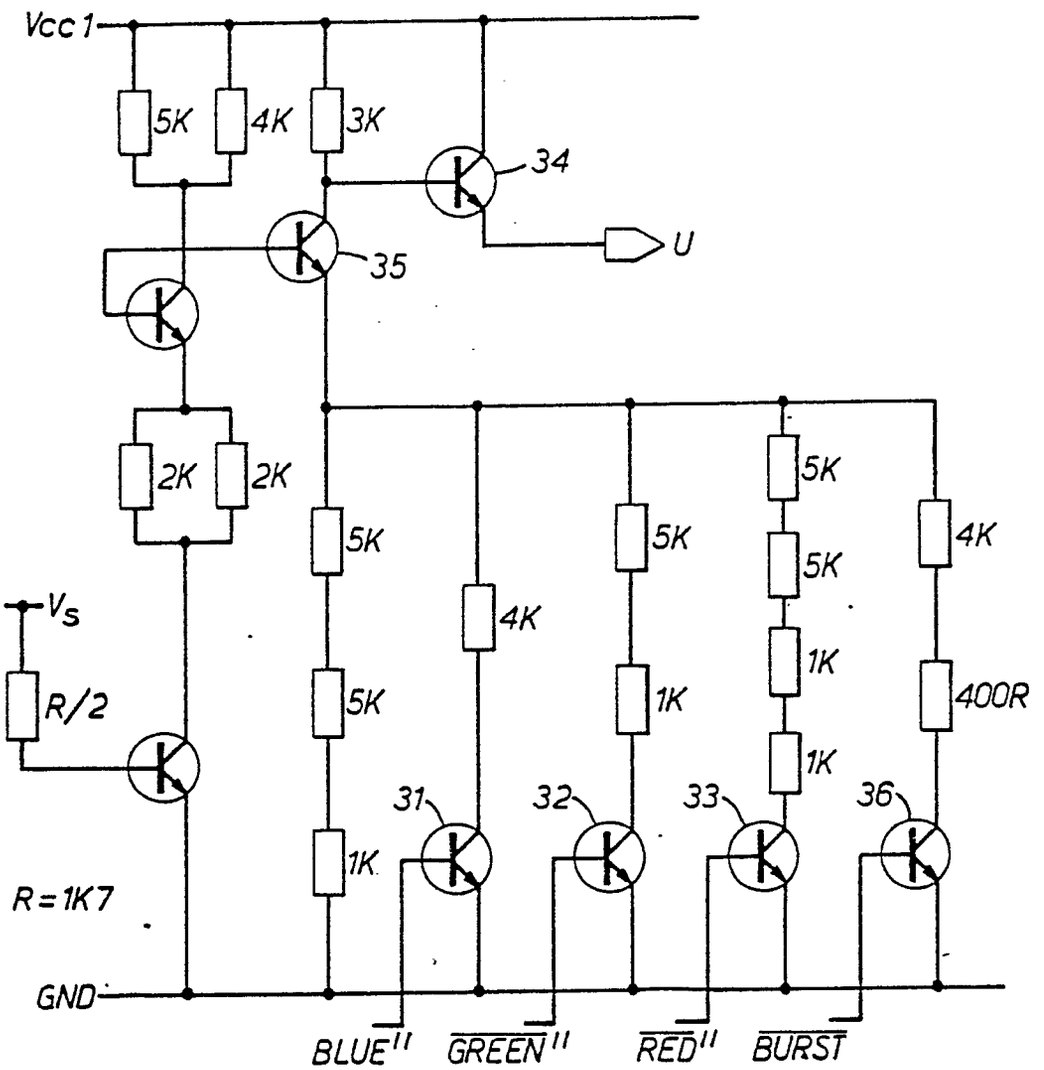

FIG. 2.

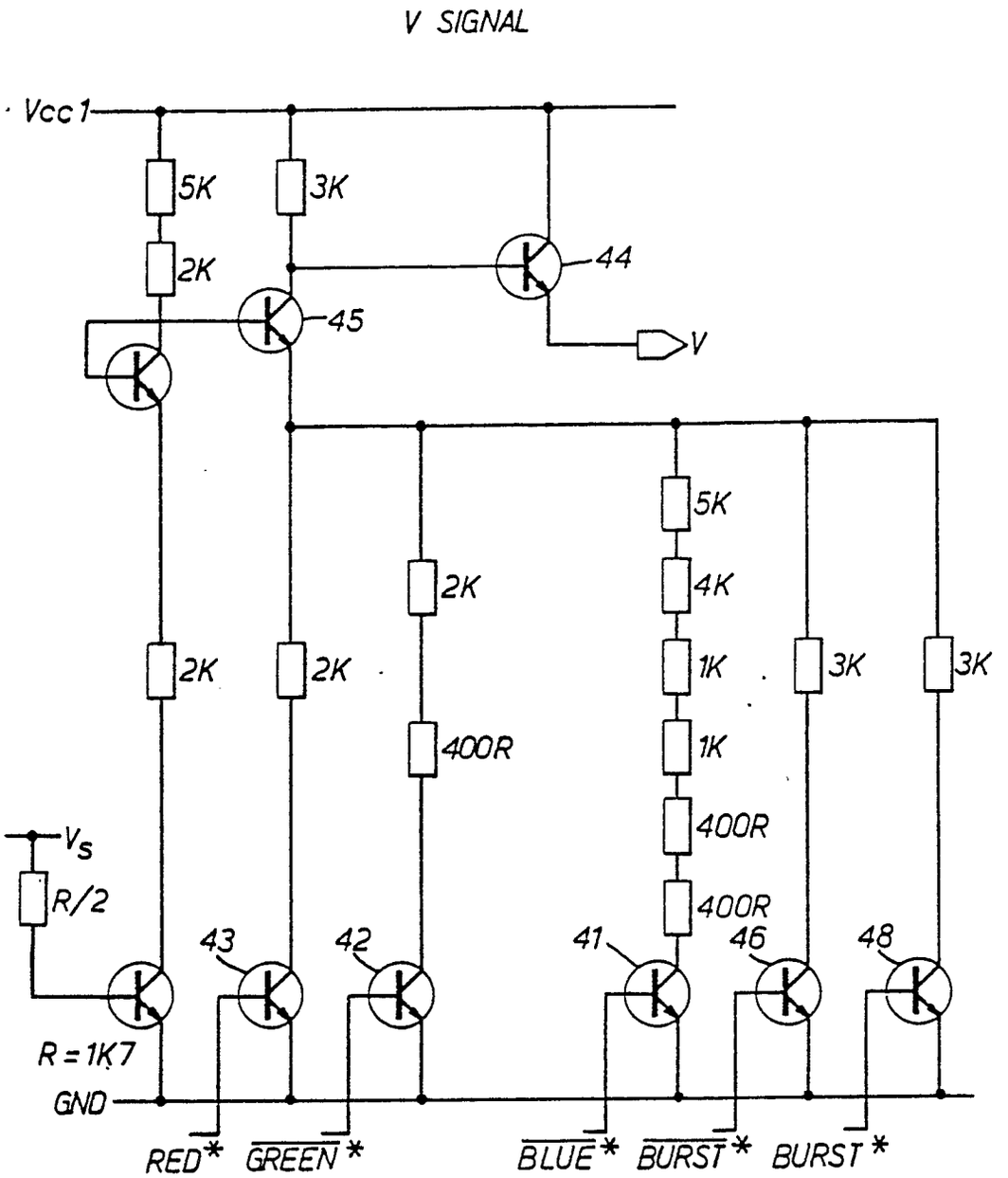
V SIGNAL
Vcc 1
5K
3K
2K
44
45
V
5K
4K
2K
1K
3K
3K
2K
2K
1K
400R
400R
400R
Vs
R/2
43
42
41
46
48
R = 1K7
GND
RED*
GREEN*
BLUE*
BURST*
BURST*

FIG. 3.

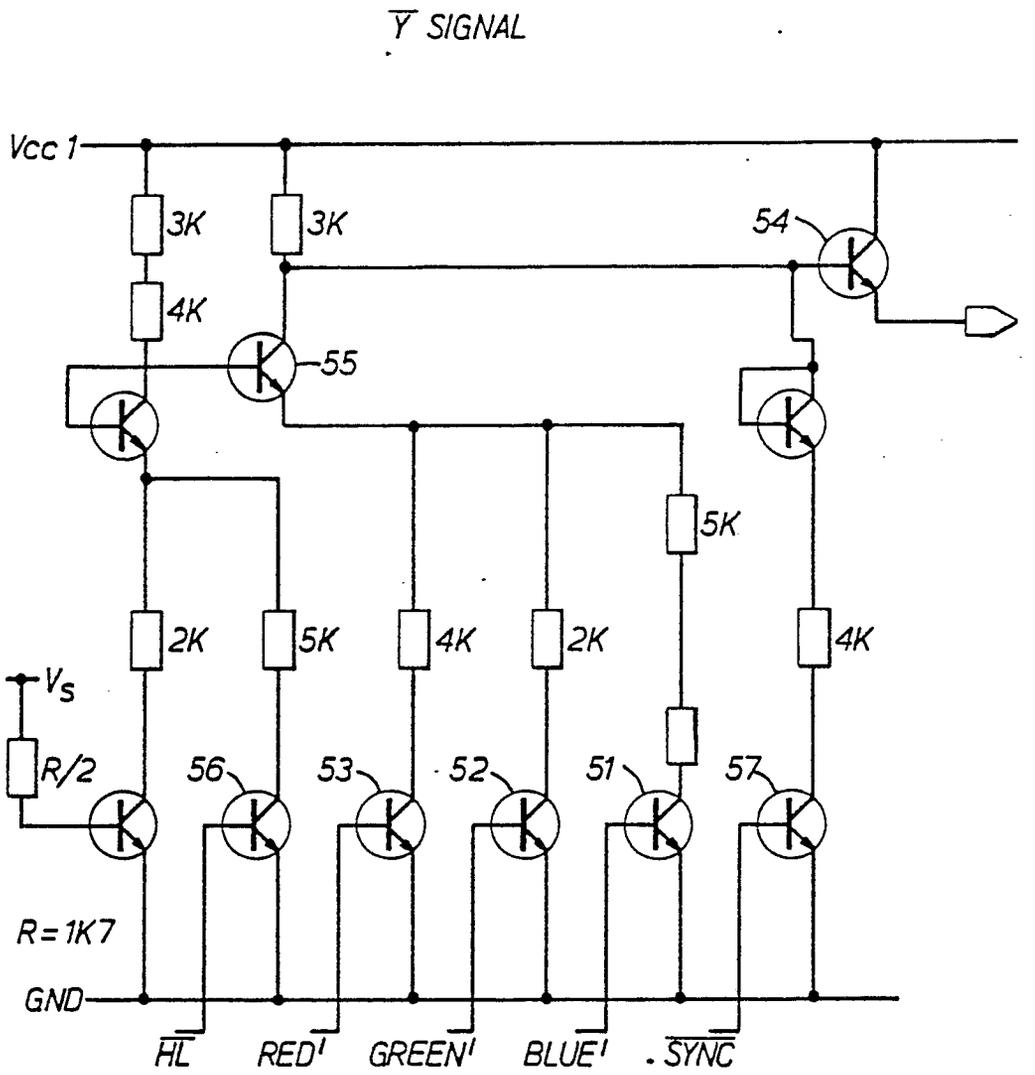
$\overline{Y}$ SIGNAL
Vcc 1
3K
3K
4K
55
54
5K
2K
5K
4K
2K
4K
Vs
R/2
56
53
52
51
57
R=1K7
GND
HL
RED'
GREEN'
BLUE'
SYNC

FIG. 4.

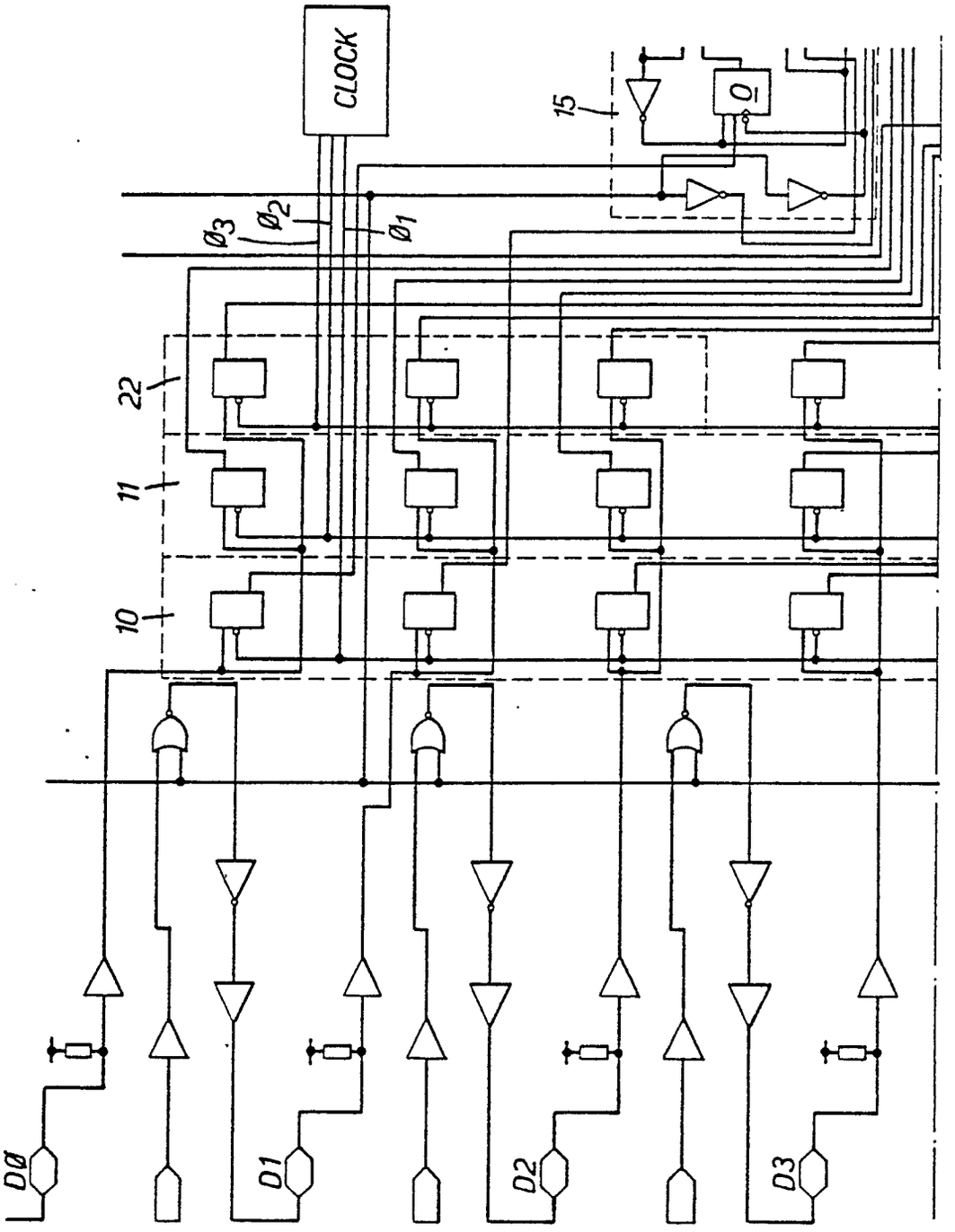

FIG. 5A-1.

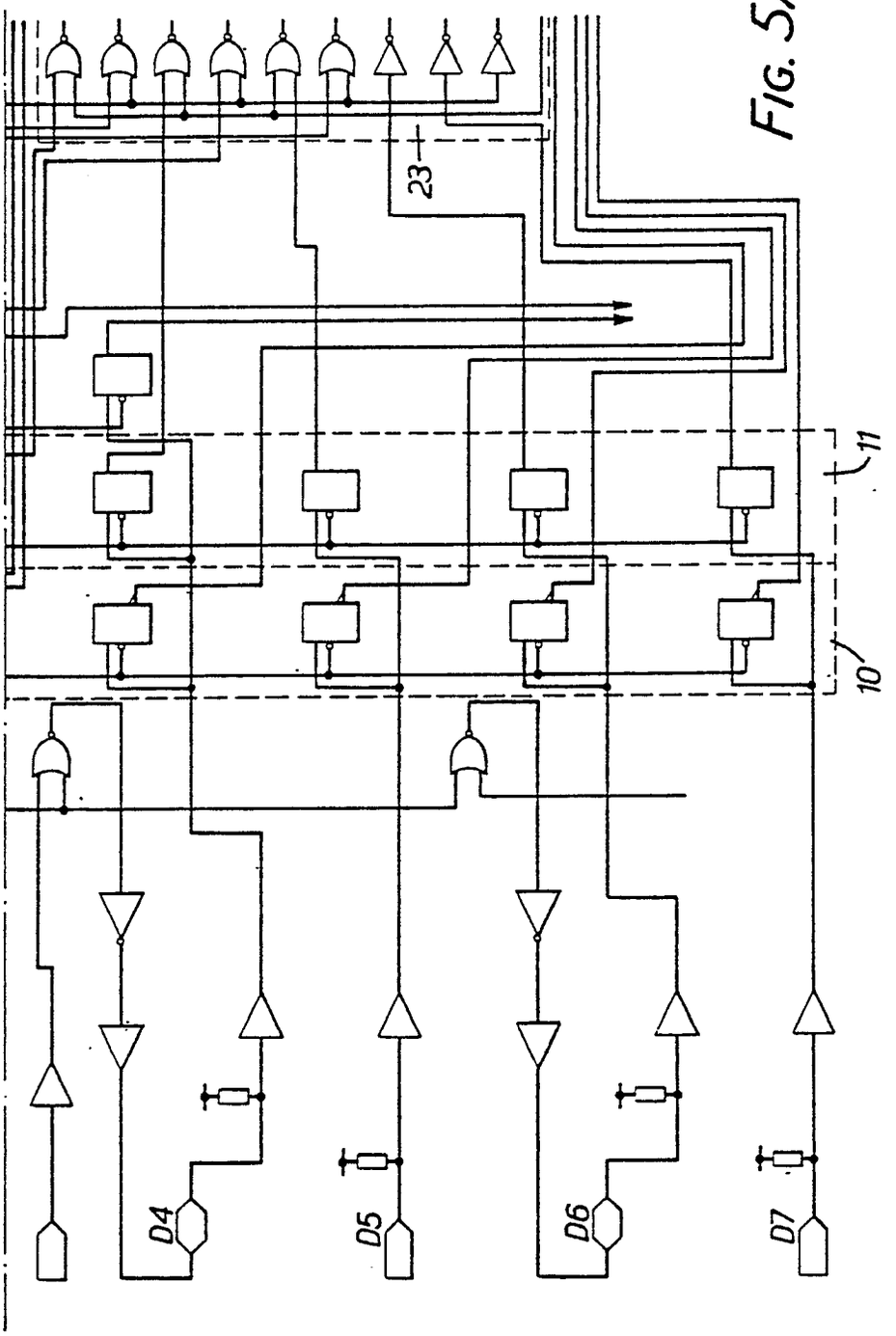

FIG. 5A-2.

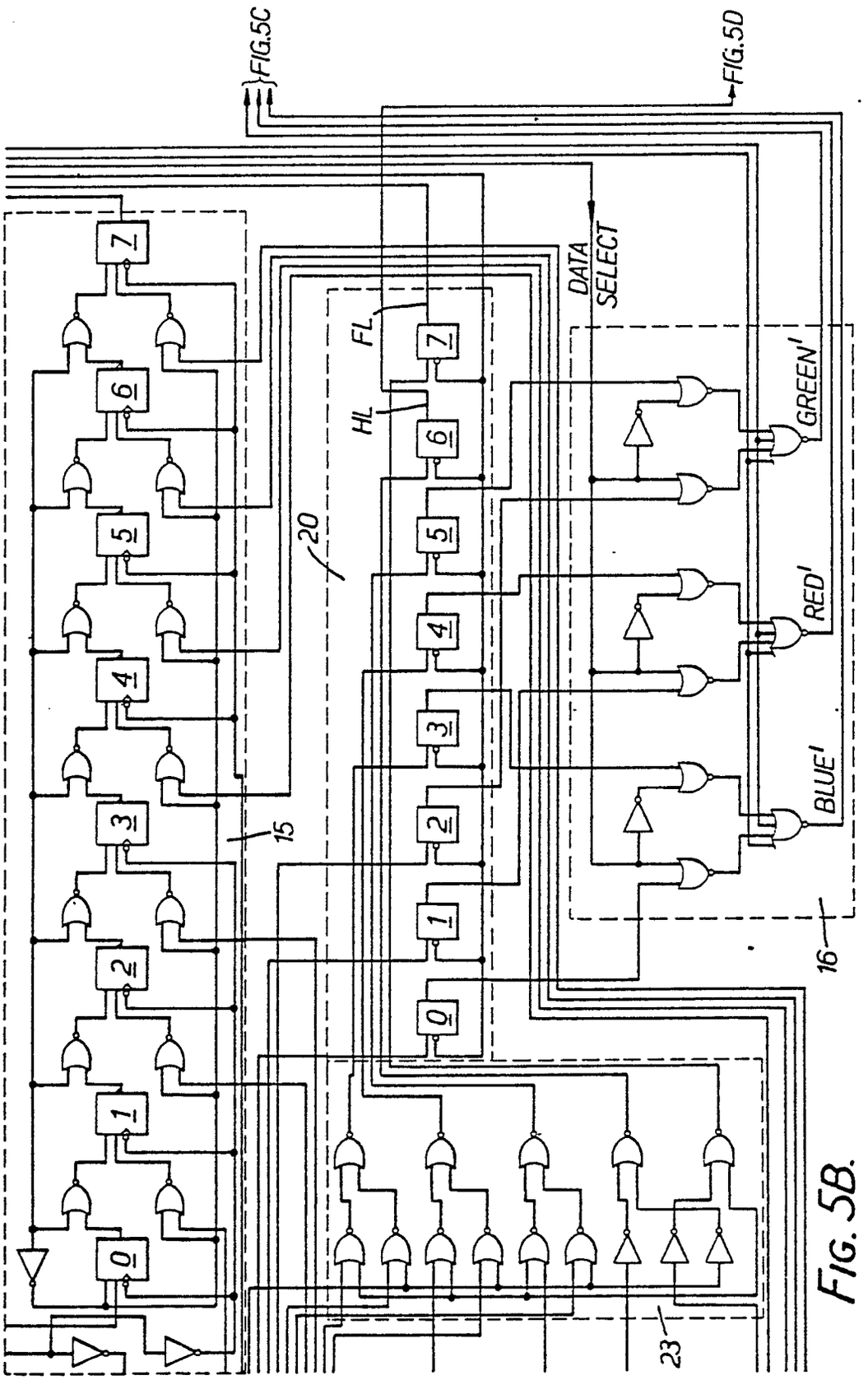
FIG.5C
FIG.5D
DATA SELECT
FL
HL
GREEN'
RED'
BLUE'
20
15
16
23
0
1
2
3
4
5
6
7

FIG. 5B.

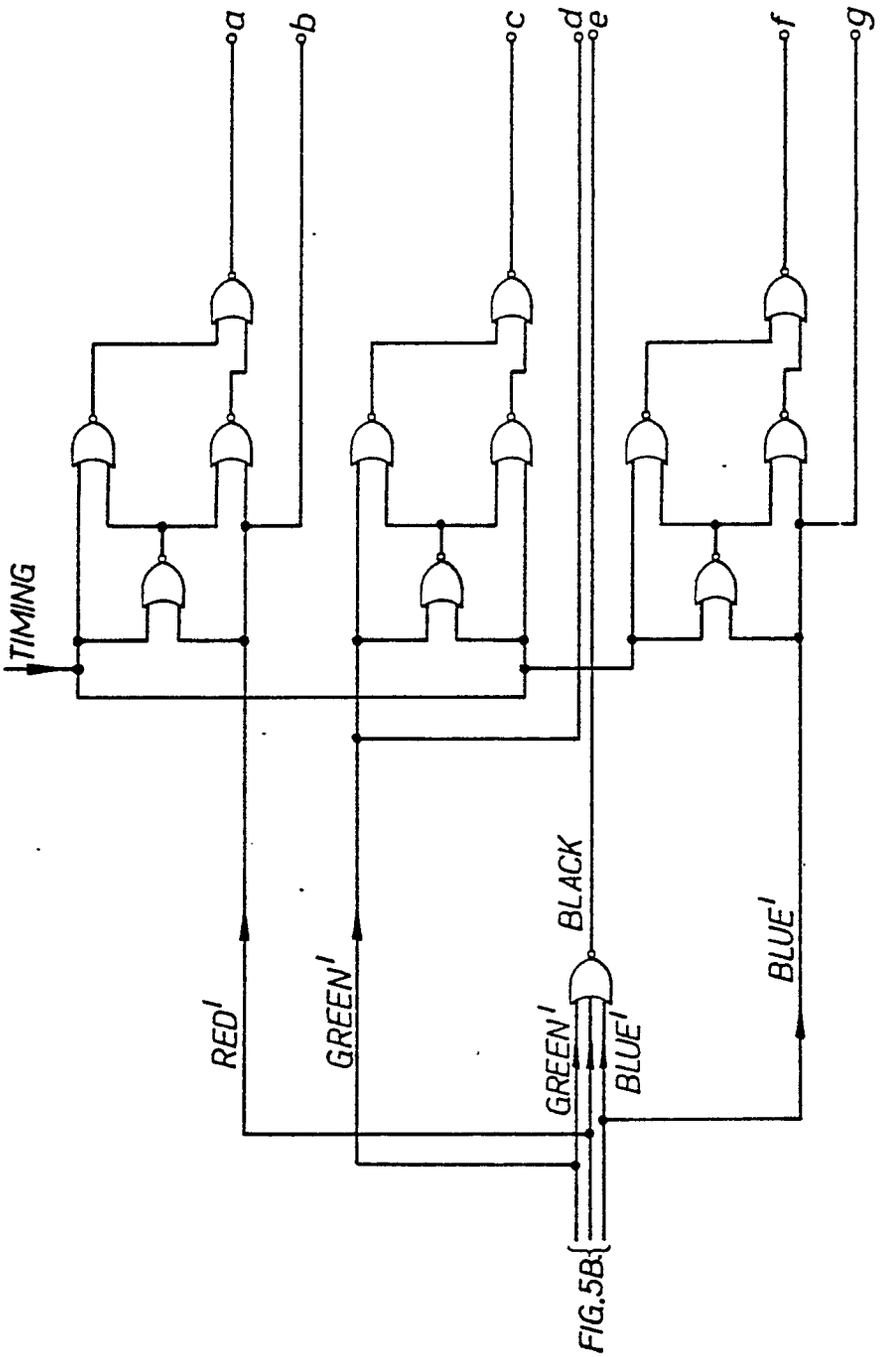

FIG. 5C.

FIG. 5D.

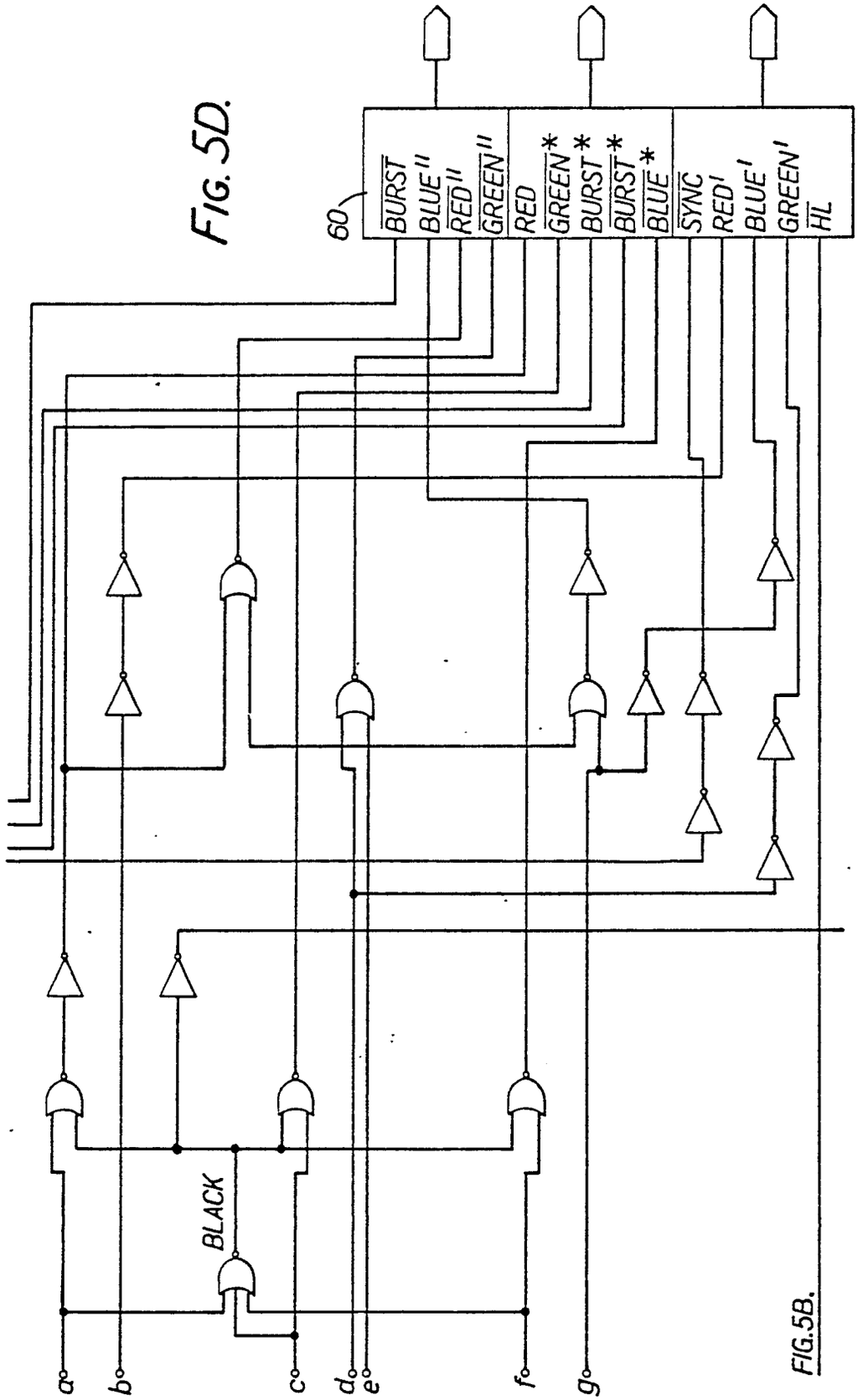
60
BURST
BLUE''
RED''
GREEN''
RED
GREEN*
BURST*
BURST*
BLUE*
SYNC
RED'
BLUE'
GREEN'
HL
BLACK
a
b
c
d
e
f
g

FIG.5B.