IV. BIPOLAR PROM PROGRAMMING INSTRUCTIONS

A. Programming the 3601 (or 3601-1)

The 3601 may be programmed using the basic circuit of Figure 1. Address inputs are at standard TTL levels. Only one output may be programmed at a time. The output to be programmed must be connected to V_{CC} through a 300Ω resistor. This will force the proper programming current (3-6mA) into the output when the V_{CC} supply is later raised to 10V. All other outputs must be held at a TTL low level (0.4V).

The programming pulse generator produces a series of pulses to the 3601 V_{CC} and CS_2 leads. V_{CC} is pulsed from a low of 4.5 ± .25V to a high of 10 ± .25V, while CS_2 is pulsed from a low of ground (TTL logic 0) to a high of 15 ± 0.5V. It is important to accuractly maintain these voltage levels, otherwise, improper programming may result. The pulses applied must maintain a duty cycle of 50 ± 10% and start with an initial width of 1 (± 10%) μs, and increase linearly over a period of approximately 100ms to a maximum width of 8 (± 10%) μs. Typical devices have their fuse blown within 1ms, but occasionally a fuse may take up to 400ms. During the application of the program pulse, current to CS_2 must be limited to 100mA. The output of the 3601 is sensed when $\overline{CS_2}$ is at a TTL low level output. A programmed bit will have a TTL high output. After a fuse is blown, the V_{CC} and $\overline{CS_2}$ pulse trains must be applied for another 500μs. The characteristics of the pulse train are shown in Figure 2.

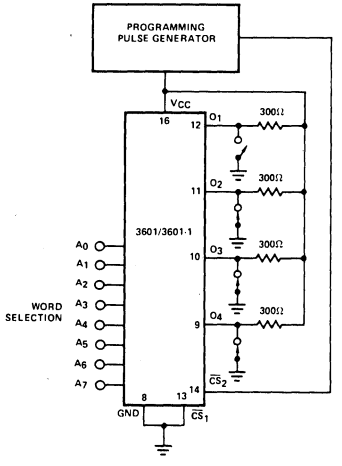

Figure 1. 3601 Programming.

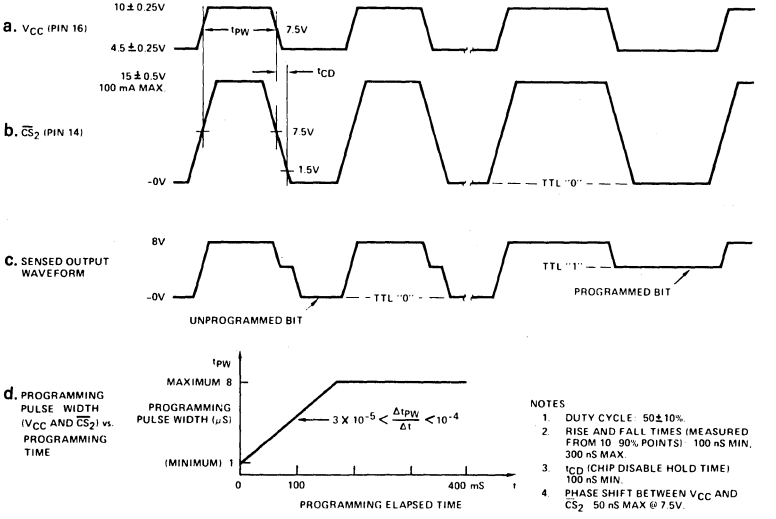

Figure 2. Pulses During Programming.

B. Programming the 3621, 2K, and 4K Bipolar PROM Families

The Intel® 3621, 2K and 4K bipolar PROMs families are programmed using the basic circuit of Figure 1. Initially all bits are in a logic 1 (high) state. Only one output may be programmed at a time. The programming current (5mA ± 10%) is forced into the output to be programmed by a current source. The current should be clamped to V_{CC} by a silicon diode. All other outputs must be allowed to float such that the outputs are allowed to rise one diode above V_{CC} (12.5V).

For simplicity of the programming description, reference will be made only to V_{CC}, however, this term includes both the V_{CC1} and V_{CC2} of the 4K PROM. There is only one V_{CC} for the 3621 and 2K PROMs. Programming pulses must be applied to both V_{CC} and $\overline{CS}$. A series of pulses is applied to the V_{CC} and $\overline{CS_1}$ (or $\overline{CS_2}$ for the 3621) leads as shown in Figure 2a and 2b respectively. The pulse applied must maintain a duty cycle of 50 ± 10% and start with an initial width of 1 (±10%) μs, and increase linearly over a period of approximately 100ms to a maximum of 8 (±10%) μs. Typical devices have their fuse blown within 1ms, but occasionally a fuse may take up to 400ms. During the application of the program pulse, the V_{CC} current must be limited to 600mA and the $\overline{CS_1}$ current to 150mA. A programmed bit will have a TTL low level. After a fuse is blown, the V_{CC} and $\overline{CS_1}$ pulse trains must be applied (the pulse width still linearly increasing to a maximum of 8μs) for another 500μs.